# Silicon nanowire field effect transistors to probe organized neurons networks

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**Abstract**
We present the fabrication and characterization of silicon nanowire field effect transistors (SiNW-FETs). Electrical behaviour of the devices are compared with 2D simulations that estimate the expected conductance modulation assisted by electrical field effect for operation in liquid environment. Then, we demonstrate the neurons growth and differentiation in vitro and their efficient coupling to the SiNW-FETs arrays.

## 1 Introduction

Neurons are excitable cells and electrical recording offers a privileged access to neuronal activity. To analyze the overall activity of neuronal networks it is crucial to record from many points of the network at once. Several methods have been developed to enable such multisite recording. They are either based on voltage sensitive or calcium sensitive dyes, extracellular micro electrode arrays or CMOS technologies for field potential recording. Silicon nanowire field effect transistor is the only configuration that has recently offered the sensitivity, length scale and timescale required to monitor neuronal activity at a sub-cellular level. Top-down technologies using Silicon-On-Insulator substrates have in parallel demonstrated their ability to detect some biological signals like DNA hybridization and pH variations, suggesting their potential use for cellular signal detection.

We present electrical characterization of field effect transistors made from SOI substrates. The overall nanoFET array has been designed to record and stimulate neuron networks of controlled architectures grown on top of the silicon chip. One example of such network will be presented.

## 2 Methods

Field effect transistors are fabricated by etching the 50 nm-thick silicon top layer of a SOI substrate oriented (100). The doping concentration of the top Si layer is $10^{21}$ at./cm$^3$ (Boron implantation) at the metal-silicon junction and a10 µm width ribbon in which the nanowire is etched remains non-implanted.

Contacts lines are made to address each nanowire by deposition of titanium (20 nm) and gold (60 nm) on a resist-patterned surface, followed by the lift-off of the resist. An aluminum hard mask hides the nanowire during the etching process. This hard mask is made by aluminum deposition and the lift-off of an electron beam lithography patterned resist. The following structure was been obtained by reactive ion etching of the uncovered silicon (figure 1).

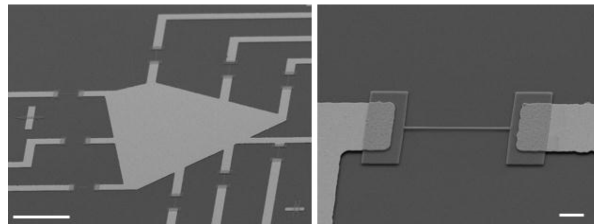

**Fig. 1.** Electron beam micrographs of 100 nm wide Si-NWFETs (right) integrated in a triangular array (left). The design is chosen to follow the spike propagation along a closed triangular neurons network (Fig.5). Scale bars are 40 µm (left) and 1µm (right).

Then a thick oxide (typ. 200 nm-thick-parylen-C or Silica) is deposited to electrically isolate the contact lines during liquid operations. Oxide is then removed above silicon nanowires by RIE etching while the rest of the chip is protected with a DUV resist pattern (figure 2, left). The resist is then removed and a thin gate oxide (typ. 5-20 nm thick $HfO_2$ or $Al_2O_3$ ) is deposited by atomic layer deposition to cover and isolate the nanowires (Figure 2, right).

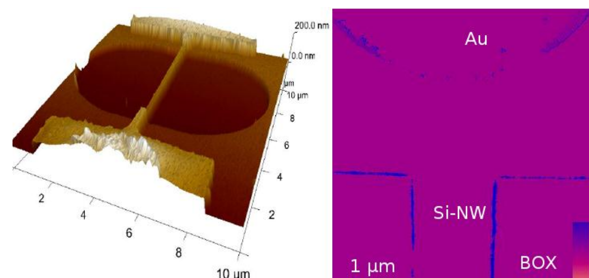


**Fig. 2.** Left. Atomic force micrograph of the final SI-NW device. Source and drain are covered by a thick oxide (Parylen or $SiO_2$) that is removed on the top of the Si-NW. Right. Tunneling atomic force micrograph of a connected Si-NW covered with a thin front gate oxide (5nm, alumina). Color scale is 1V, current-voltage converter gain is 10mV/pA.

A rapid thermal annealing at 500°C is performed before oxide deposition in an inert Ag/H atmosphere without oxygen-gases. The annealing induced a titani-

um silicide alloy on top of the contacts [1,2] that forms a conductive layer with a low Schottky barrier height. Before annealing, nanowires exhibit a resistance higher than 10MΩ, while it is reduced to 300kΩ after the annealing. The resistance has been reduced by almost 30 times.

## 3 Results and discussion

The drain source current-voltage ($I_{DS}$-$V_{DS}$) characteristic curves are measured by changing the voltage bias of the nanowires while the drain to source current is recorded.

First, modulation of the nanowire conductance is measured as function of a back gate voltage (fig.3) applied on the Si-substrate forcing charge accumulation at the Si/buried oxide (200nm thick) interfaces. The leakage current through the buried oxide is controlled with a picoampermeter (typically few pA).

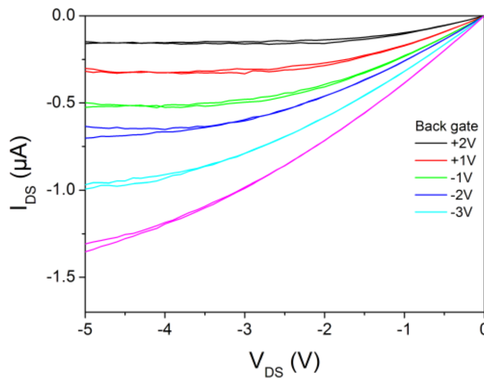


**Fig. 3.** Drain source current $I_{DS}$ as function of the applied drain source voltage $V_{DS}$ for several back gate voltage applied on the Si substrate.

Then, we investigate the response of the SiNW-FETs to voltage spikes applied in a front side physiological environment. An accurate control of the solution potential could be achieved with a three-probes potentiostat experiments. For these applications the nanowires conductance are measured with a home-made electronics card of 12 parallel acquisition inputs with a 200µs average measurement time allowing stable long time recordings [3].

These experiments are compared with 2D numerical experiments performed with commercial software (Silvaco). These allow rapid estimations of the expected conductance modulation with a liquid front gate, for several parameters such as doping concentration and device geometry. Figure 4 shows the expected conductance of a 30 nm thick, $10^{19}$ at./cm$^3$ boron doped Si-ribbon as a function of the front gate voltage, and the corresponding carriers distributions in the depletion regime.

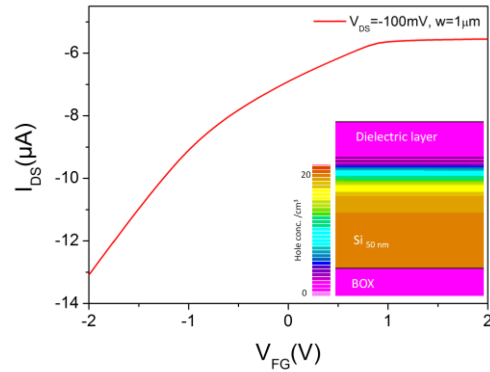


**Fig. 4.** 2D simulation of the drain source current as function of a front gate applied voltage. A dielectric layer ($e_r$~78.5) of same dielectric constant than water replaces the front side solution. Inset shows the layers stack and the hole concentration distribution in the depletion regime.

Finally, in vitro neurons networks are achieved with poly-lysine polymer patterns made on the SiNW-FETs with conventional lift-off process. The PLL polymers allow neurons adhesion and growth, while the PLL pattern geometry generates mechanical forces on the neurites that control the axonal differentiation (fig.5) [4]. Accurate localization of the axons in the network is essential for an efficient SiNW-neurons arrays alignment aimed to follow spikes propagation.

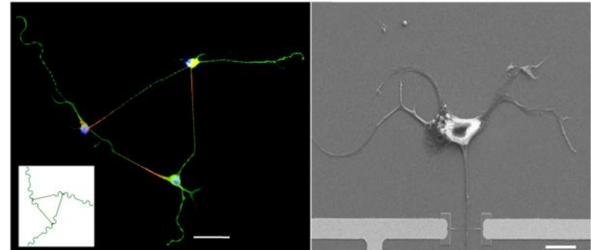

**Fig. 5**. Left. Fluorescent micrograph of a three-neurons network (6DIV). Axons are marked with a red fluorofore. The growth guidance was achieved through the use of adhesion PLL micropatterns shown with the inset. Scale bar is 50µm. Right. Scanning electron micrograph showing the efficient neurite-nanowire coupling. Scale bar is 10µm.

**Conclusion.** We have shown fabrication and characterization of SiNW-FETs arrays and their coupling to neurons networks that should be useful for in vitro neuronal signals detection. This method appears suitable to investigate signal transmission and synaptic plasticity in several network architectures.

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