Quantum Computing on Silicon
an academic POV

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Outlines

- Why silicon?
- Quantum toolbox for silicon qubit
- Perspectives for large scale

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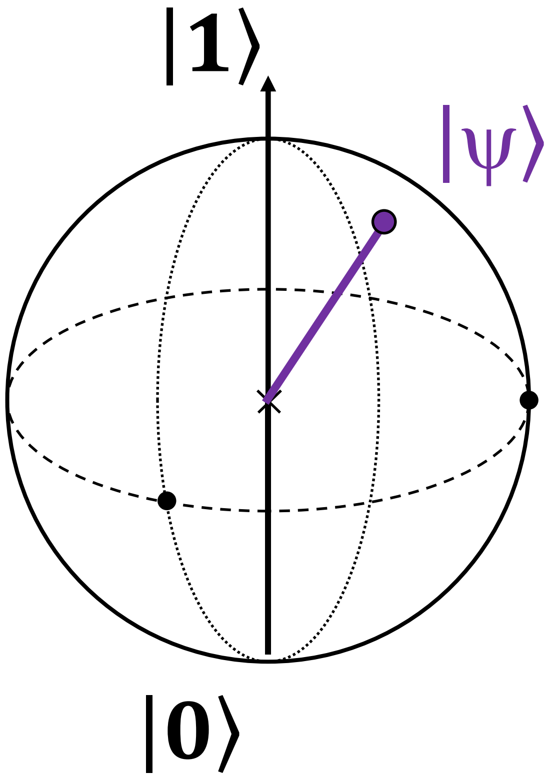
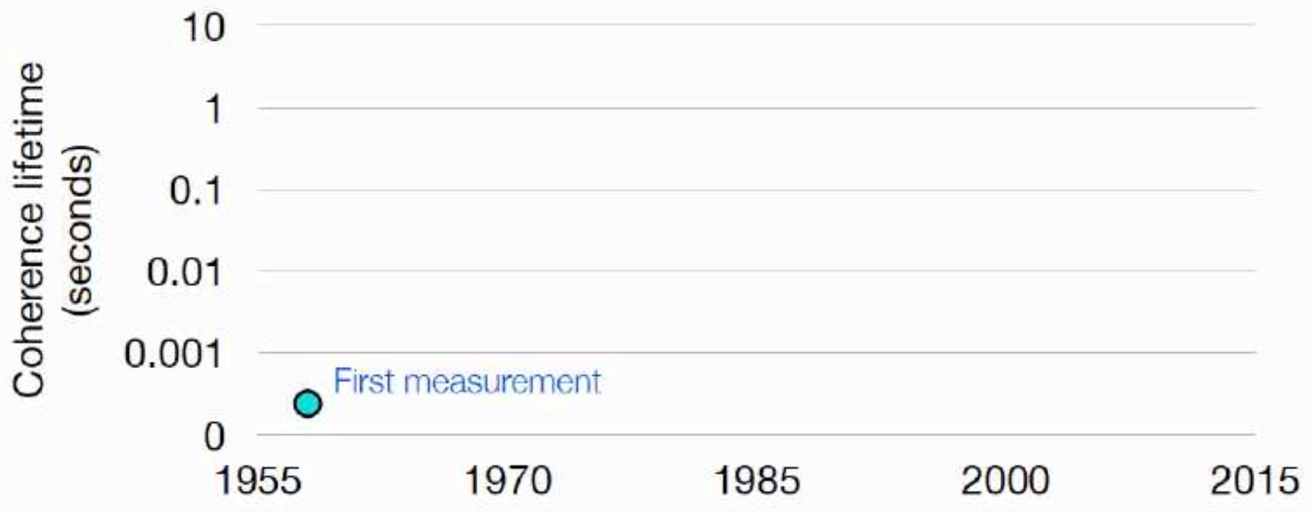
Quantum coherence



$$|\psi\rangle = a|0\rangle + b|1\rangle e^{i\varphi}$$

Quantum coherence in silicon

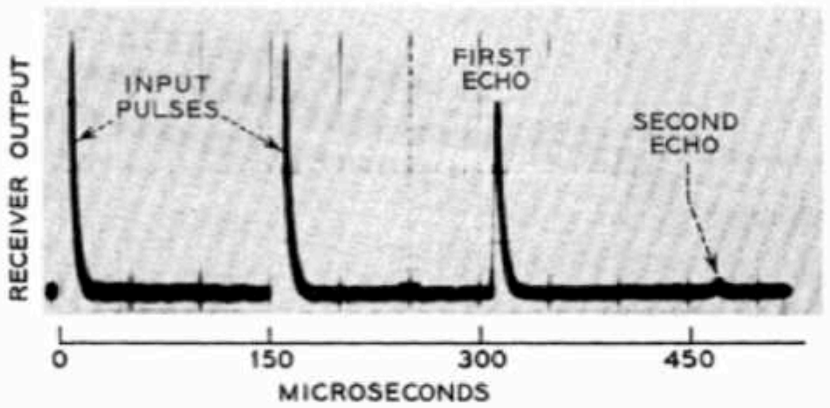


MICROWAVE SPIN ECHOES FROM DONOR ELECTRONS IN SILICON

J. P. Gordon and K. D. Bowers
Bell Telephone Laboratories,
Murray Hill, New Jersey

(Received October 9, 1958)

With the introduction of the spin-echo technique by Hahn,[1] it became possible to observe and measure directly transverse relaxation times T_2 in substances where the resonance lines involved were inhomogeneously broadened by local field variations. The spin-echo technique has

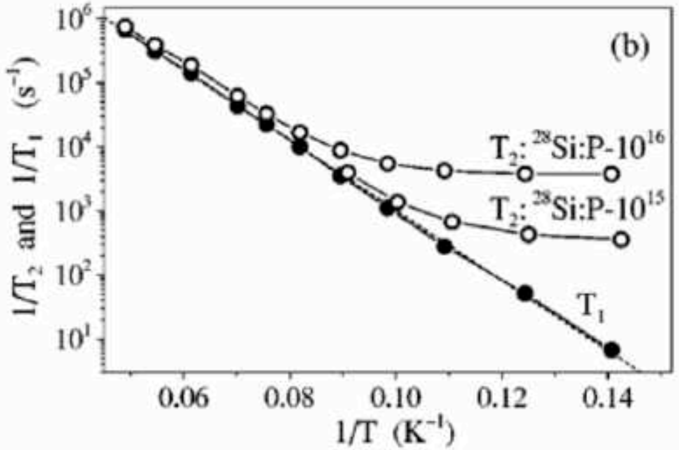


Quantum coherence in silicon

PHYSICAL REVIEW B 68, 193207 (2003)

Electron spin relaxation times of phosphorus donors in silicon

A. M. Tyryshkin,[1] S. A. Lyon,[1,*] A. V. Astashkin,[2] and A. M. Raitsimring[2]
[1]*Department of Electrical Engineering, Princeton University, Princeton, New Jersey 08544, USA*
[2]*Department of Chemistry, University of Arizona, Tucson, Arizona 85721, USA*
(Received 6 August 2003; published 20 November 2003)



Isotopic purification: ^{28}Si

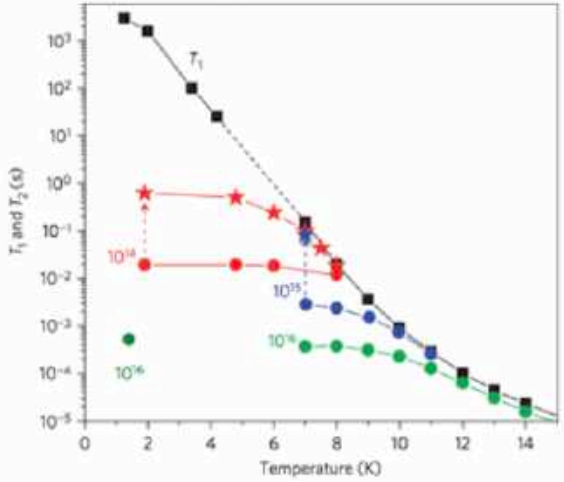
nature materials

ARTICLES

PUBLISHED ONLINE: 4 DECEMBER 2011 | DOI: 10.1038/NMAT3182

Electron spin coherence exceeding seconds in high-purity silicon

Alexei M. Tyryshkin[1], Shinichi Tojo[2], John J. L. Morton[3], Helge Riemann[4], Nikolai V. Abrosimov[4], Peter Becker[5], Hans-Joachim Pohl[6], Thomas Schenkel[7], Michael L. W. Thewalt[8], Kohei M. Itoh[2] and S. A. Lyon[1]*

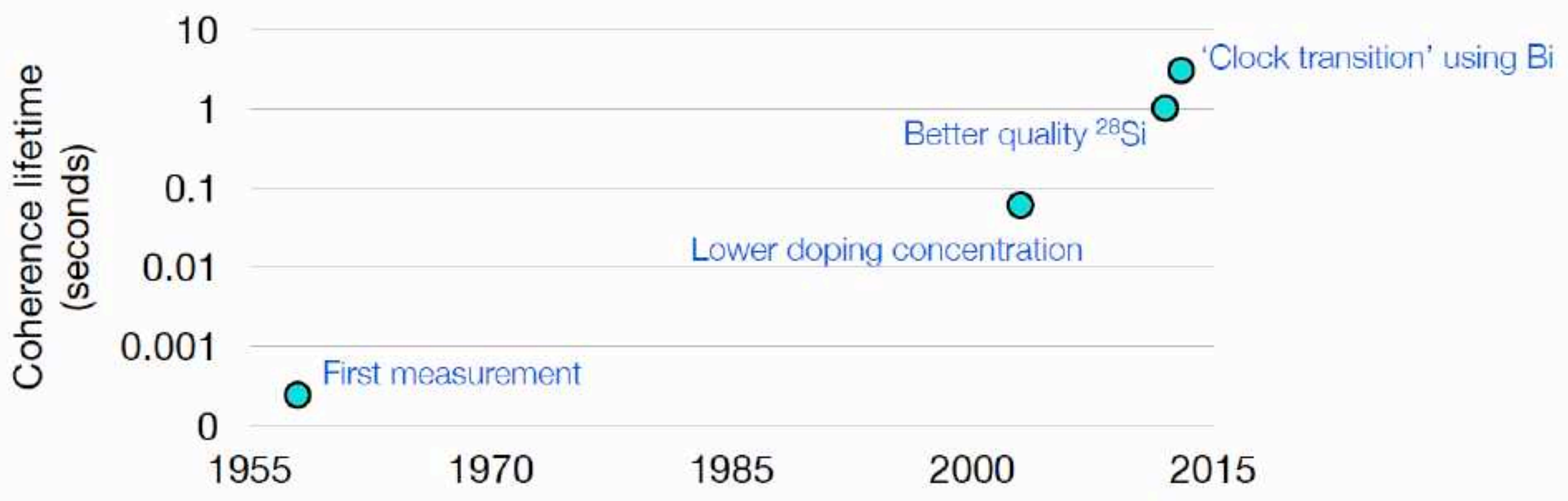


natSi

^{28}Si

^{28}Si	(92.2%)	S=0
^{29}Si	(4.7%)	S=1/2
^{30}Si	(3.1%)	S=0

Isotopic purification: ^{28}Si



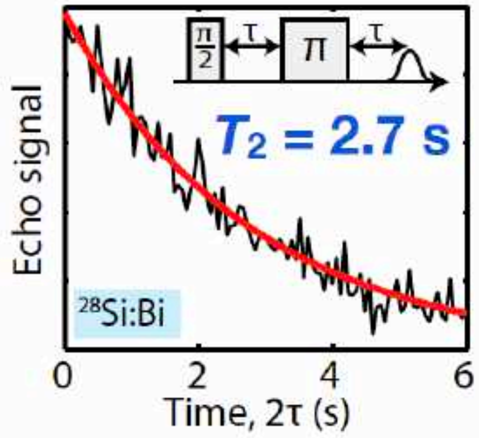

nature nanotechnology

LETTERS

PUBLISHED ONLINE: 23 JUNE 2013 | DOI: 10.1038/NNANO.2013.117

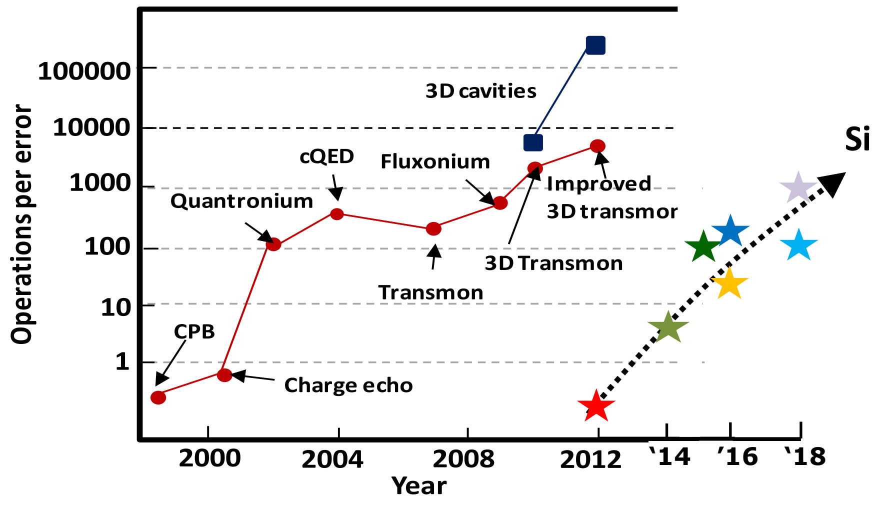
Atomic clock transitions in silicon-based spin qubits

Gary Wolfowicz[1,2]*, Alexei M. Tyryshkin[3], Richard E. George[1], Helge Riemann[4], Nikolai V. Abrosimov[4], Peter Becker[5], Hans-Joachim Pohl[6], Mike L. W. Thewalt[7], Stephen A. Lyon[3] and John J. L. Morton[1,8]*



Silicon catching up state of the art

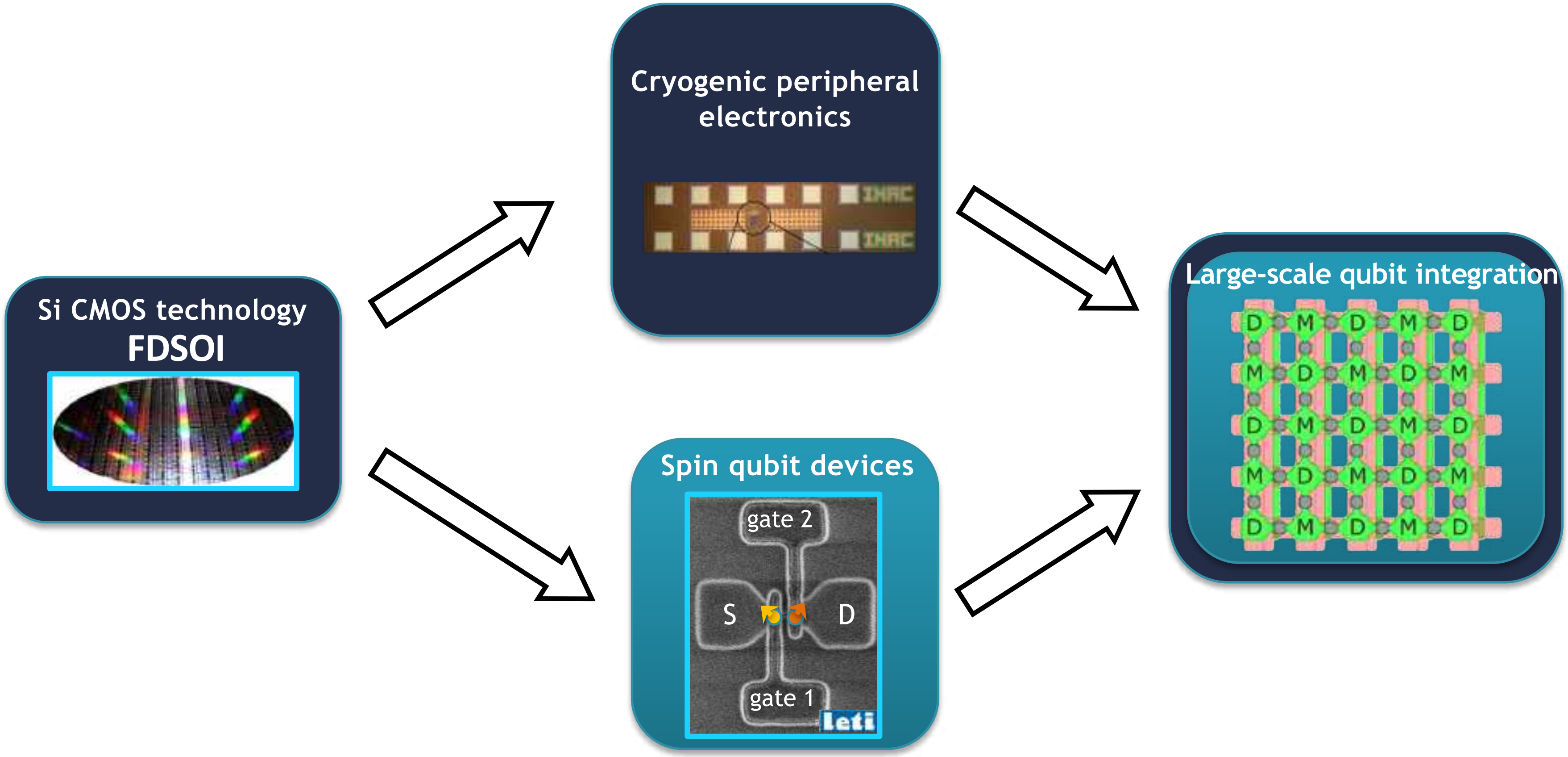
BENCHMARKING AGAINST SUPERCONDUCTING QUBITS



Adapted from M. H. Devoret, R. J. Schoelkopf, *Science* 2014

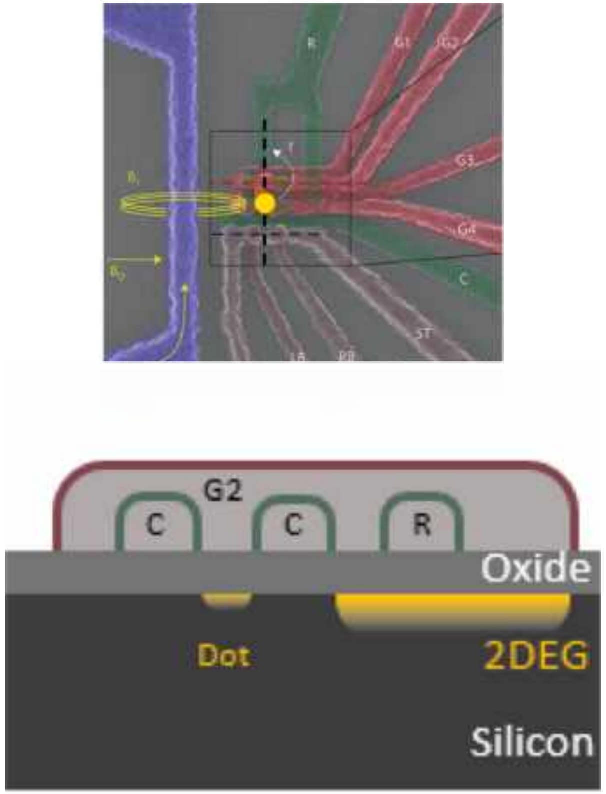
- Yoneda *et al. (RIKEN), Nature Nano 2018*: Quantum dot electron spin qubit in ^{28}Si/SiGe
- Takeda *et al. (RIKEN), Science Adv. 2016*: Quantum dot electron spin qubit in ^{nat}Si/SiGe
- Zajac *et al. (Princeton), Science 2018*: Quantum dot electron spin qubit in ^{28}Si/SiGe
- Veldhorst *et al. (UNSW), Nature 2015*: Quantum dot electron spin qubit in ^{28}Si
- Maurand *et al. (CEA), Nature Comm. 2016*: CMOS hole spin qubit in natural Si
- Kawakami *et al. (TUDelft), Nature Nano 2014:*
- Pla *et al. (UNSW), Nature 2012*: Single-donor electron-spin qubit in natural Si

Exploiting microelectronic potential



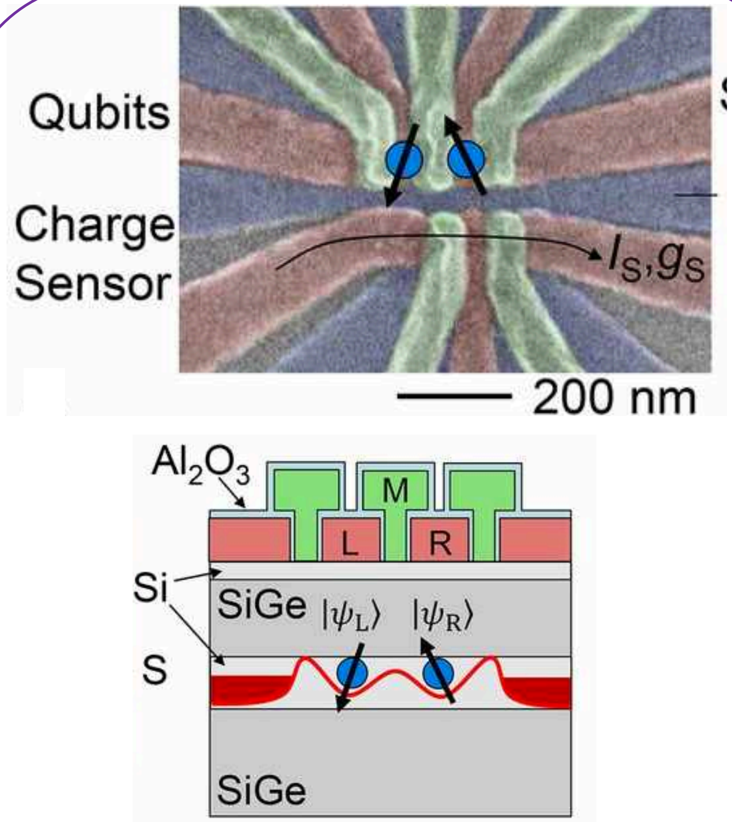
Different Si platforms

Planar MOS



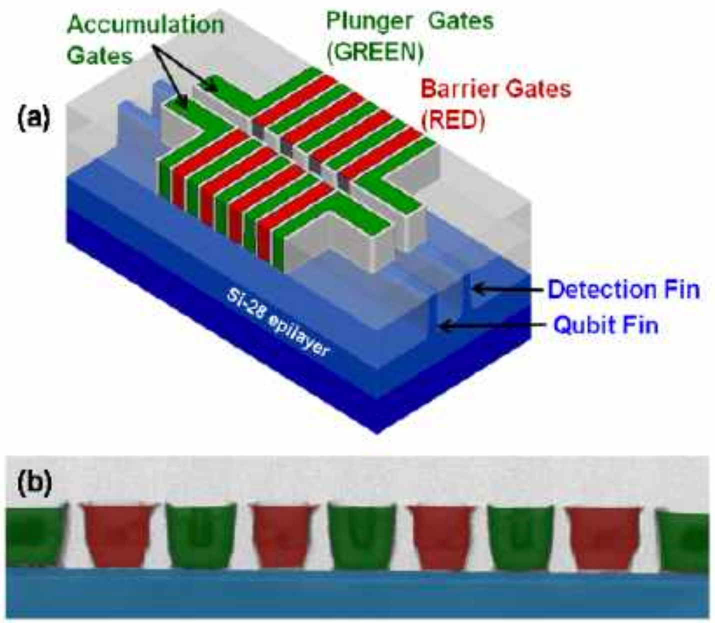
UNSW, Sandia, …

Si/SiGe



Princeton U., RIKEN, TU Delft, …

Fin-FET

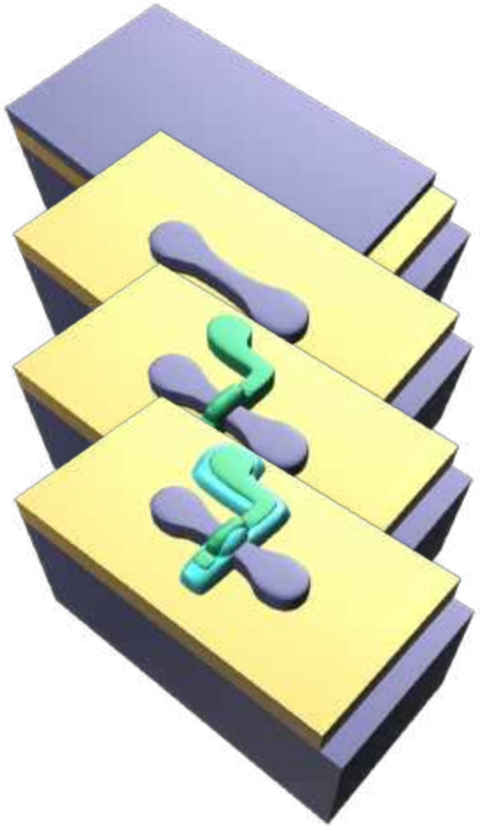


Intel - TU Delft

Grenoble nanoelectronics ecosystem

FD-SOI based devices

- 300mm SOI wafers
  T_{Si}/T_{BOx} = 12nm/145nm
- Active mesa patterning
- Thermal oxidation
- High-k/MG stack dep. & patterning
  1.9nm HfO_2/5nm TiN/50nm Poly Si
  64nm pitch
- 1st spacer
  25nm SiN
- Raised S/D epi
  18nm Si
- LDD implant and anneal
- 2nd spacer
- HDD implant and anneal
- Salicide and BEOL



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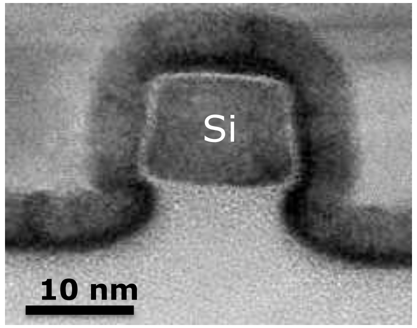
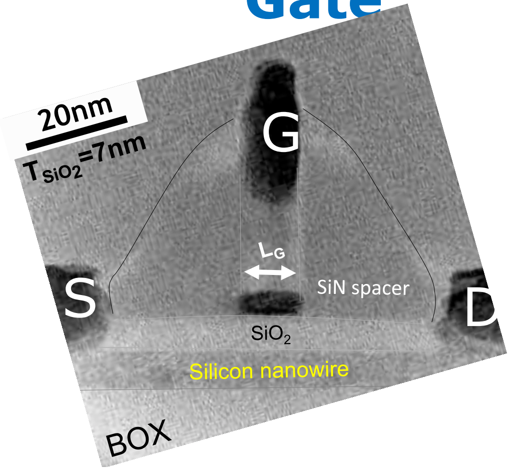


Wrap-Around Gate



Wide Spacers over thin, undoped SOI

Outlines

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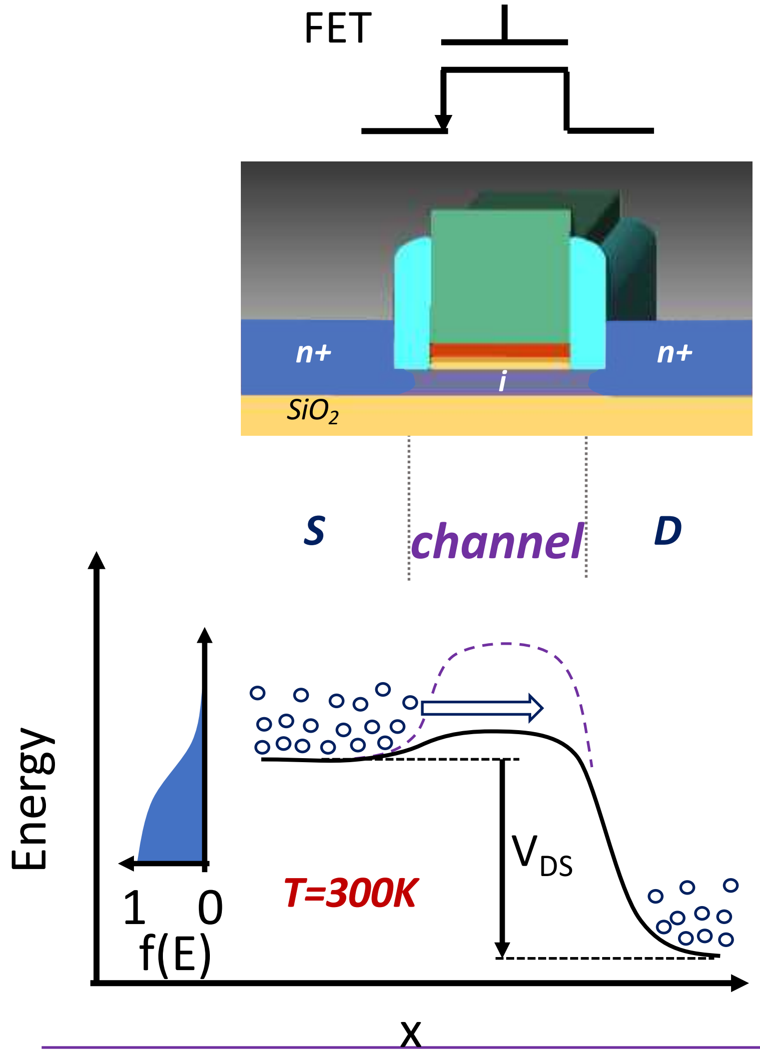
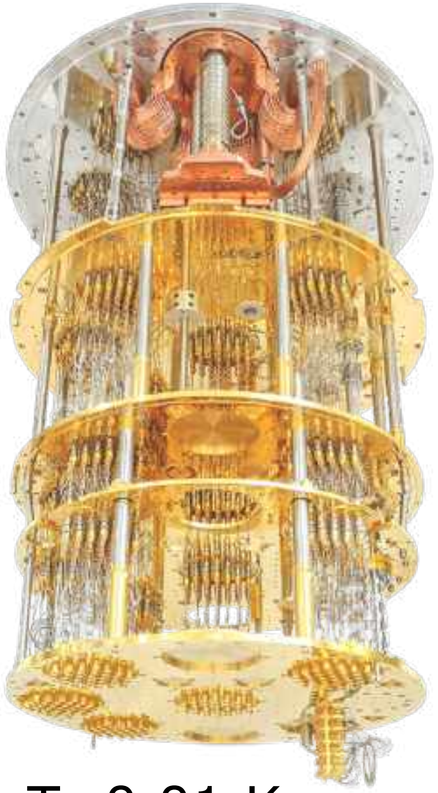
- Quantum toolbox for silicon qubit
- Perspectives for large scale

From transistors…

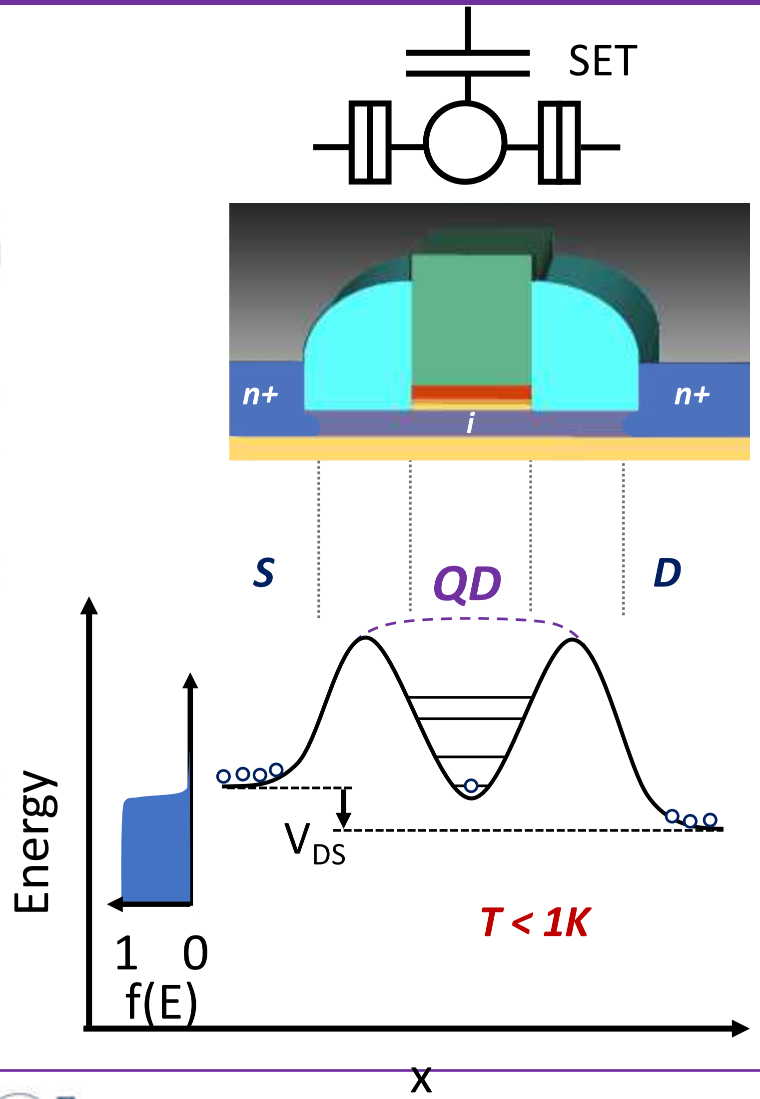


- At high temperature:
  - Carriers have significant thermal energy
  - Diffusion over the S/channel barrier when V_G is turned ON
  - Continuous flow of carriers accelerated by large V_{DS}

… to quantum dots

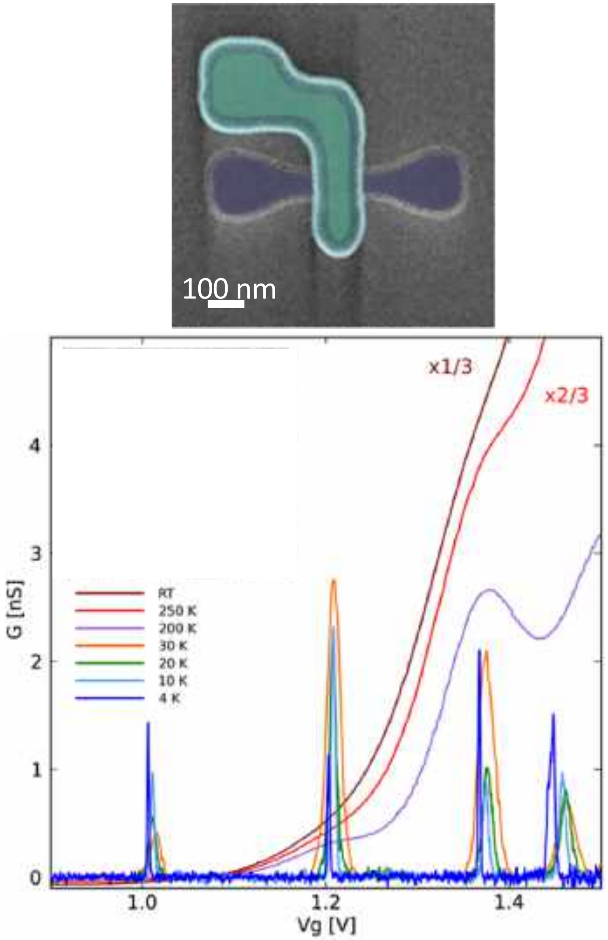


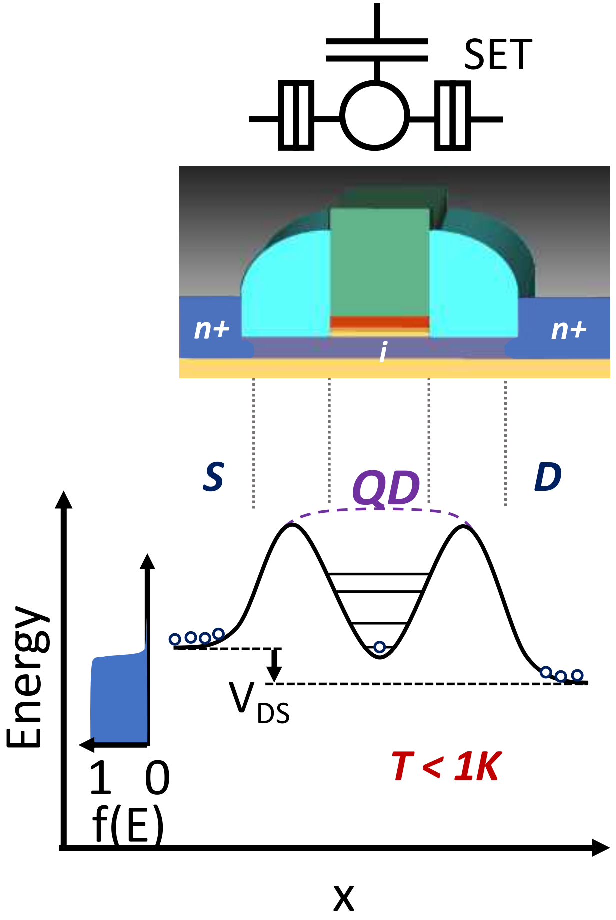
T=0.01 K



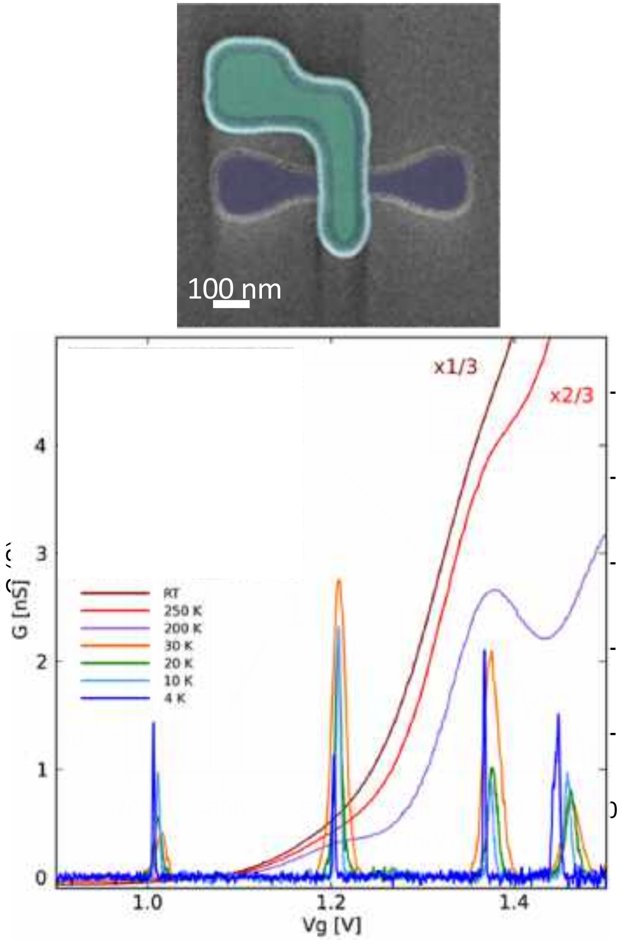
- At low temperature:
  - Wide spacers and small L_G lead to forming a well between two barriers
  - Carriers have no thermal energy and have to tunnel through
  - Energy states are quantized in the well
  - Small V_{DS} to scan precisely the resolved quantum states

Trapping a single charge

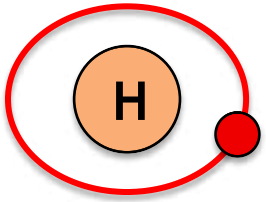




Artificial atom

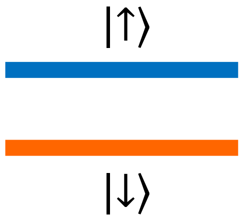


"Artificial atom"



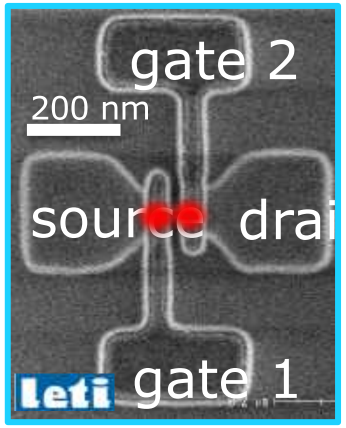
Spin S = ±1/2

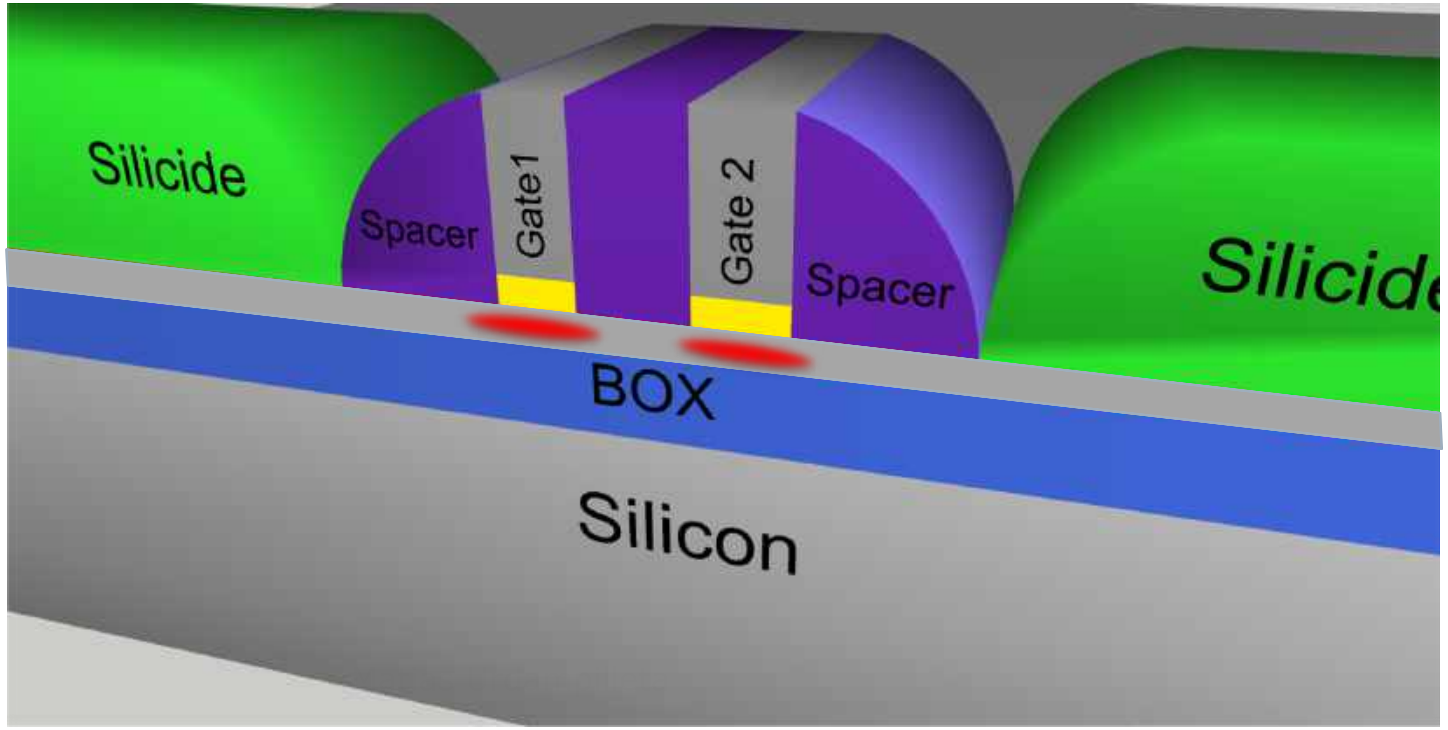
Applying a static magnetic field B, two-level spin qubit:



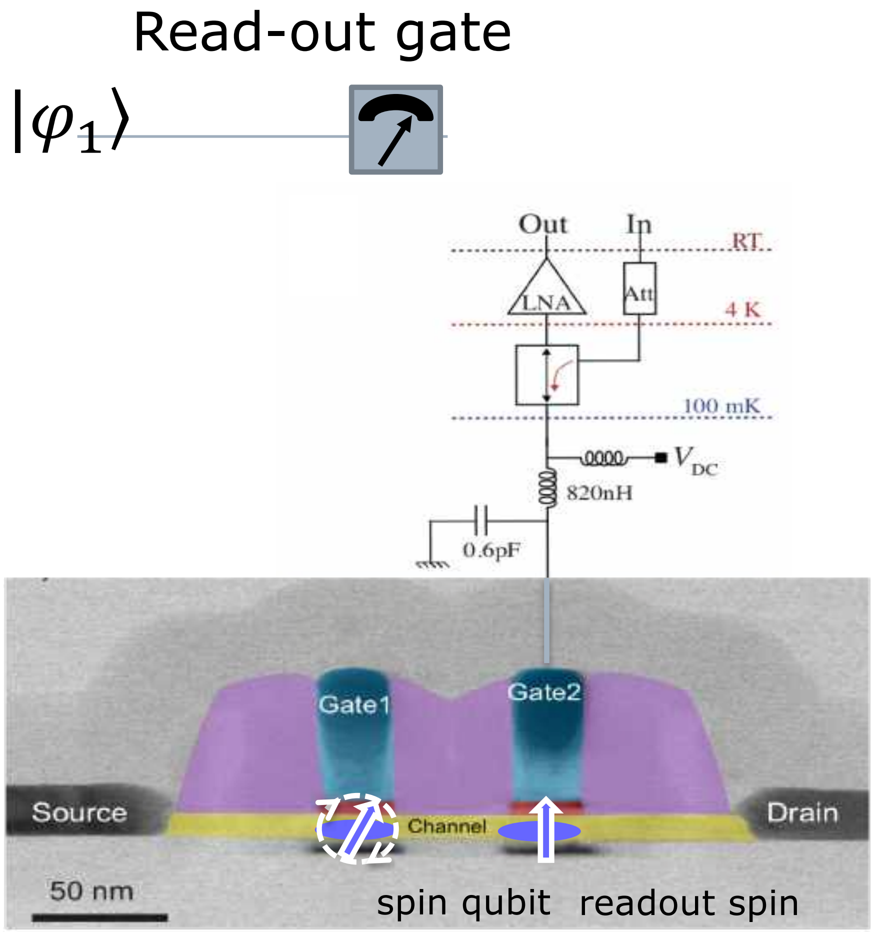
$E_Z = |g.\mu_B.B|$

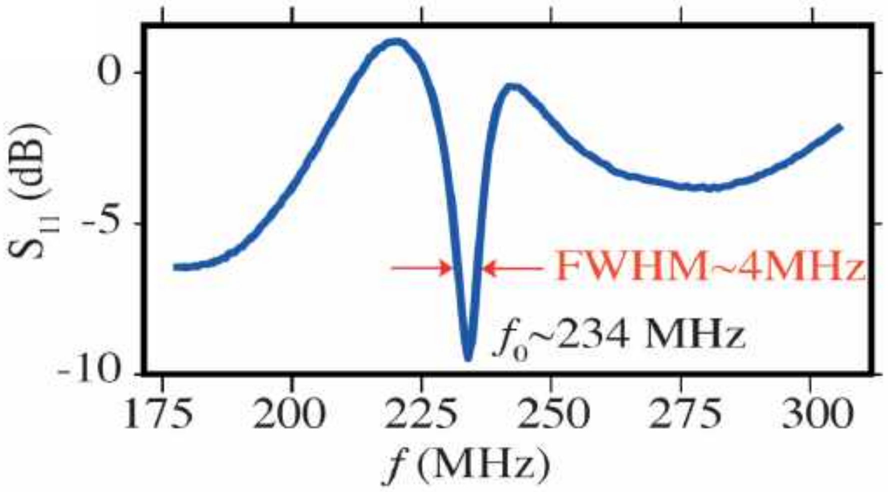
Double quantum dot

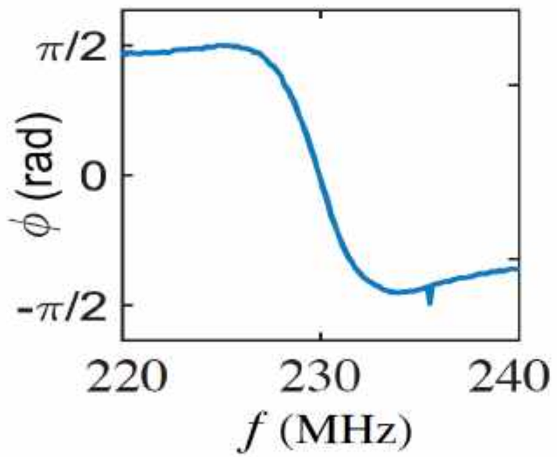




How to detect a single charge?



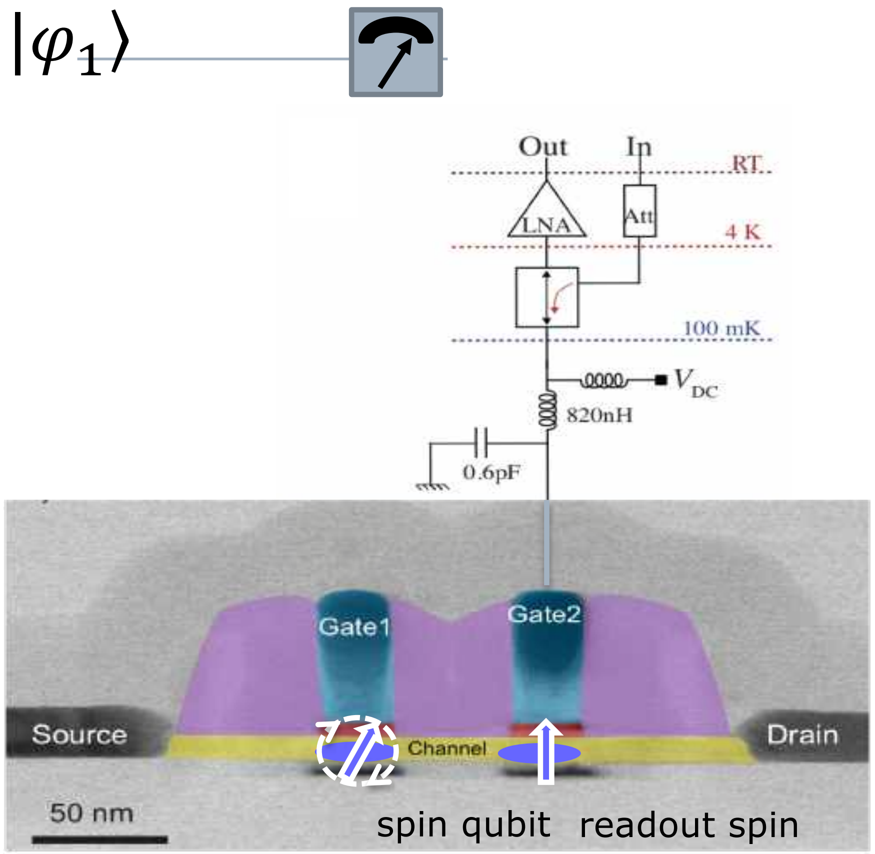


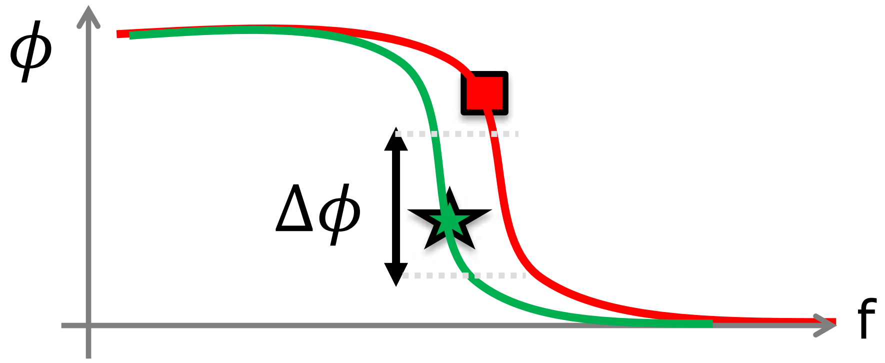


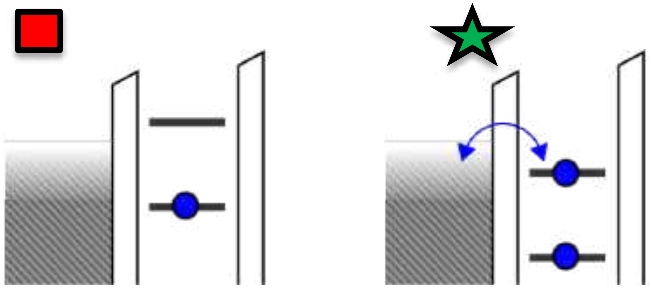
How to detect a single charge?

Read-out gate

$|\varphi_1\rangle$

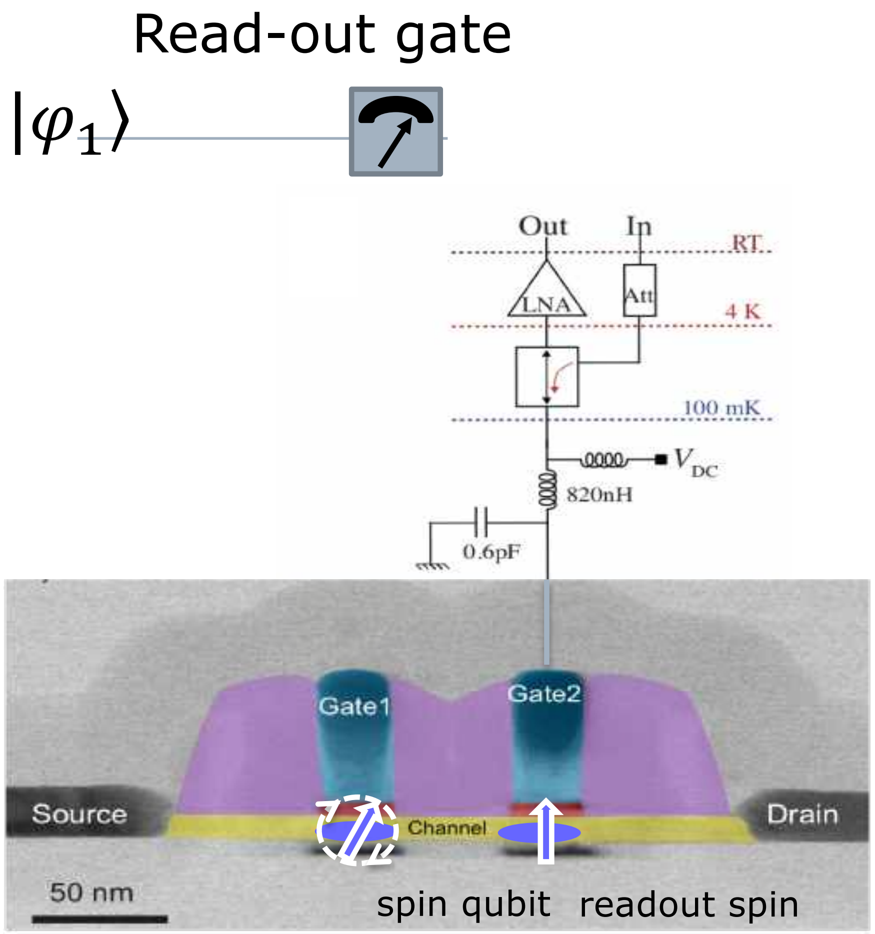


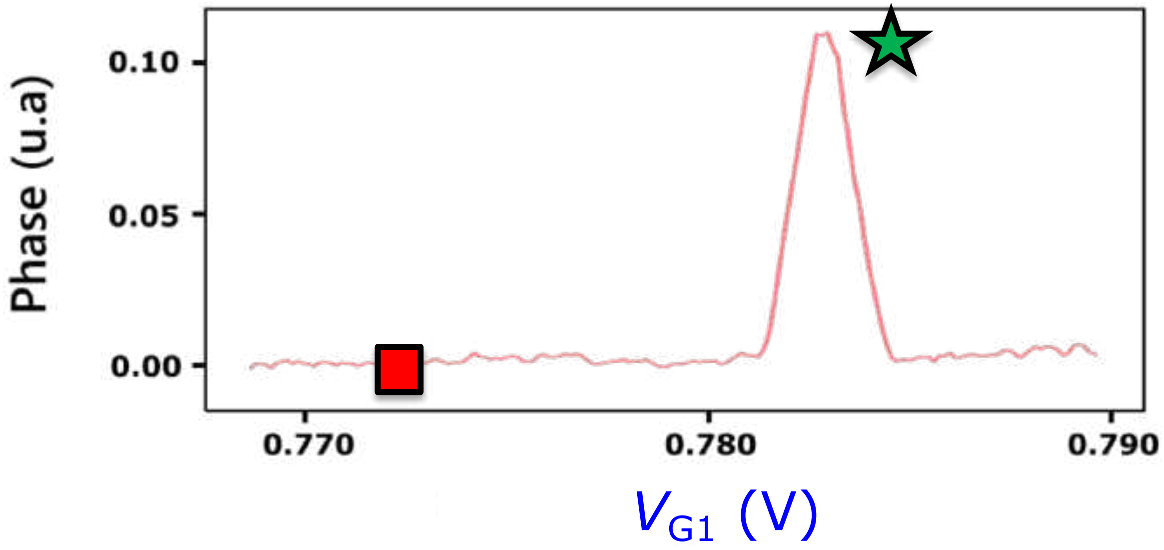


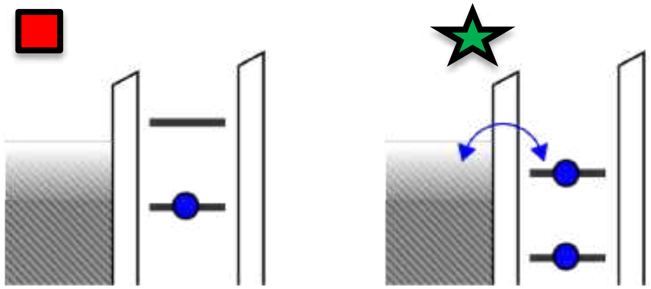


$$\Delta\phi \propto \chi_C = \frac{dQ}{dE}$$

How to detect a single charge?

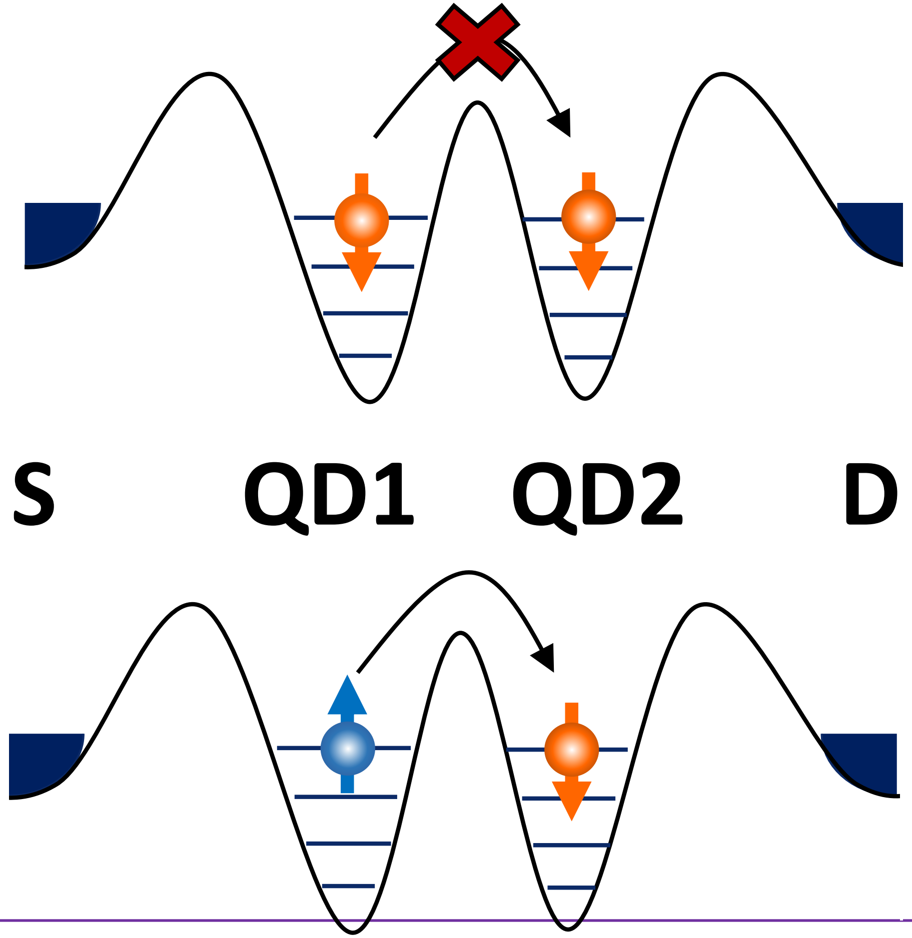






$$\Delta\phi \propto \chi_C = \frac{dQ}{dE}$$

How to detect a single spin?



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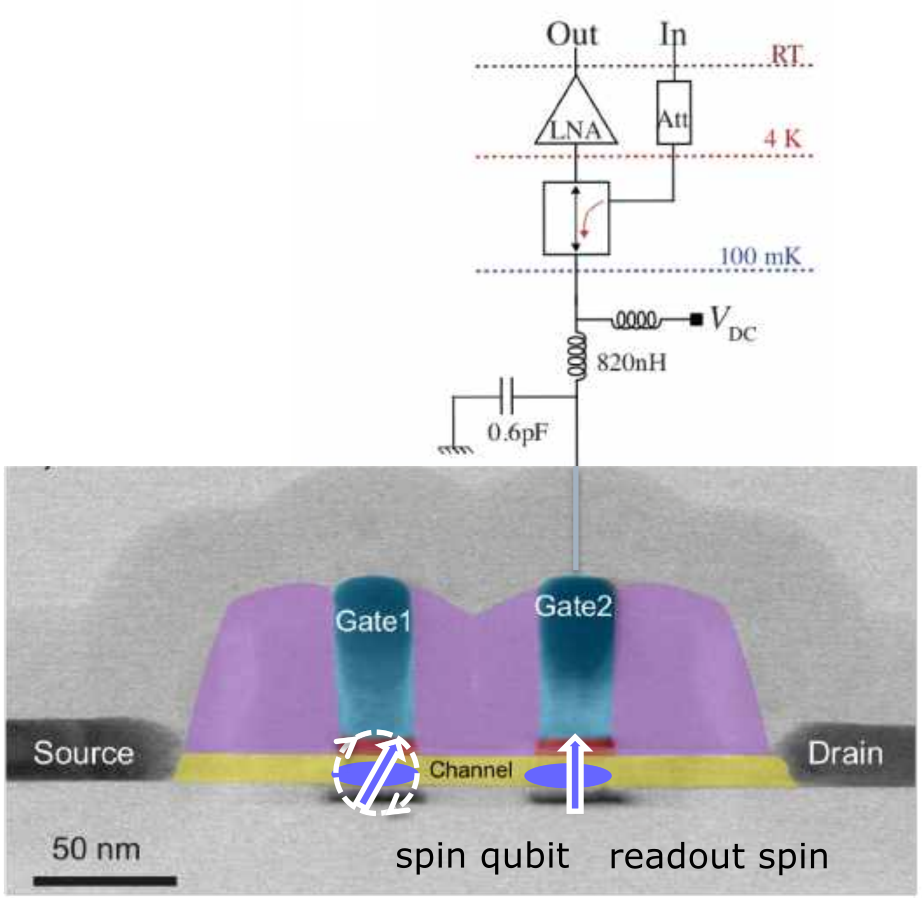
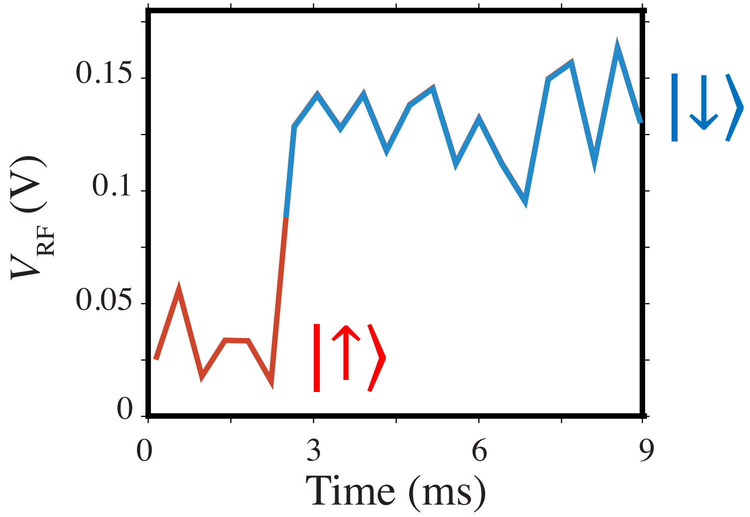
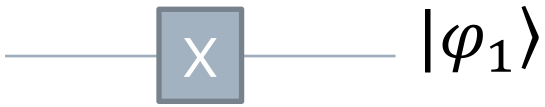




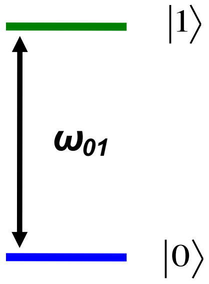
Urdampilleta et al., Nature Nano (2019)

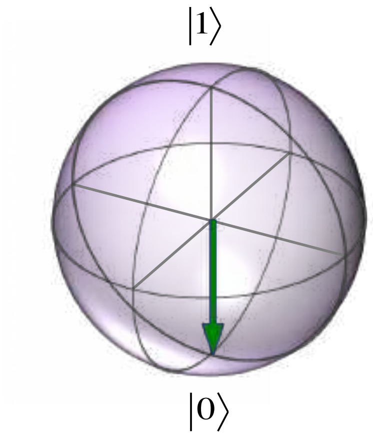
How to manipulate a single spin?

Single Qbit rotation



$\omega \propto B_{field}$





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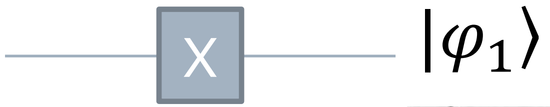
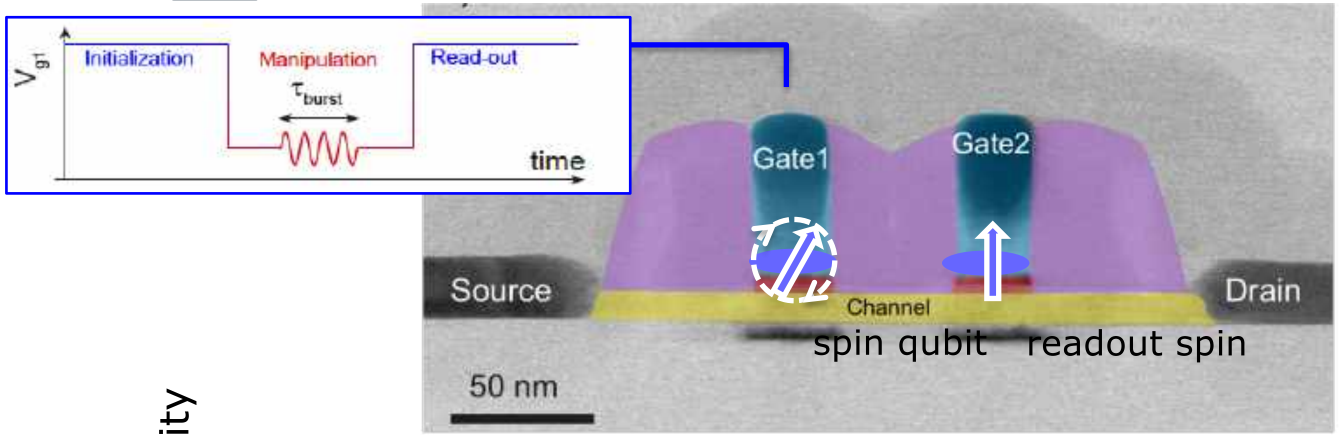
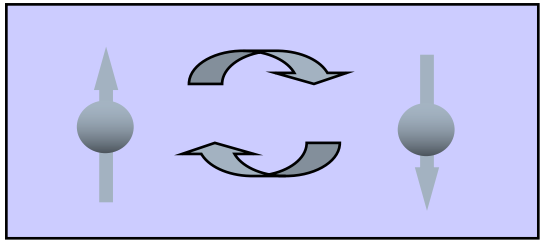
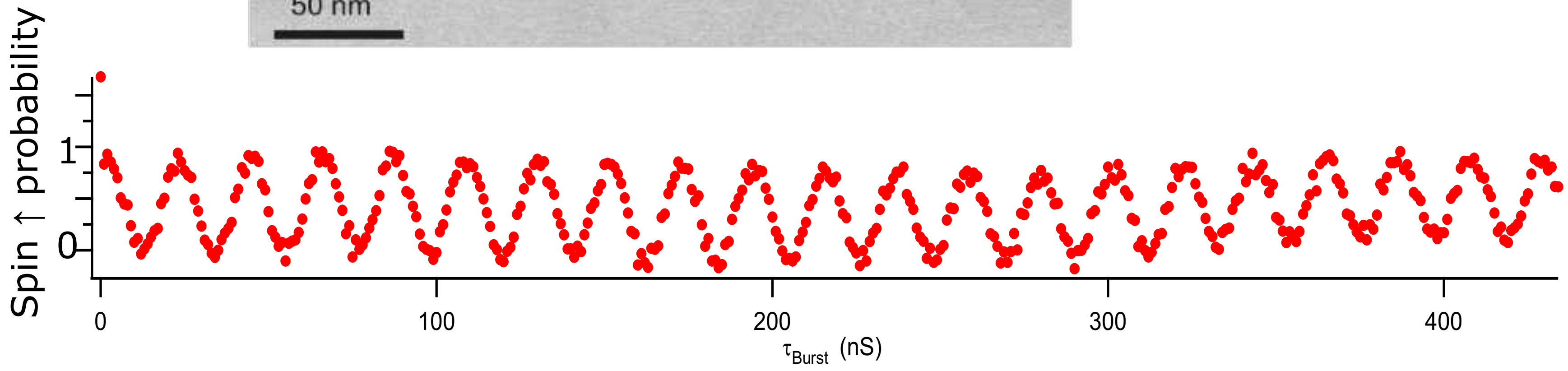




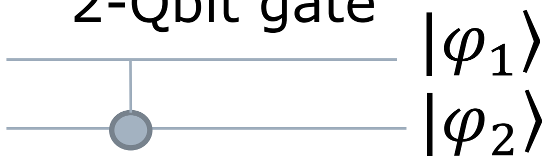




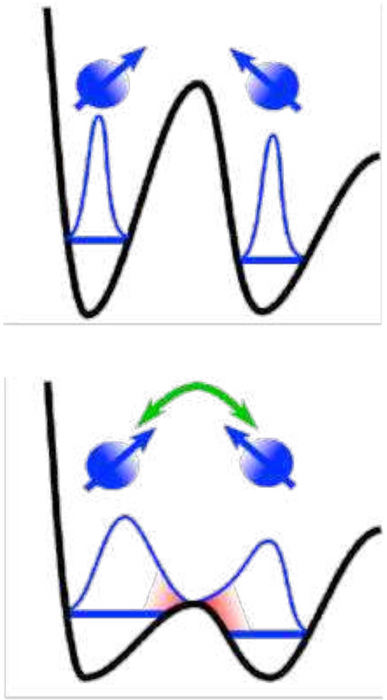
Crippa et al., Nature Commun. (2019)

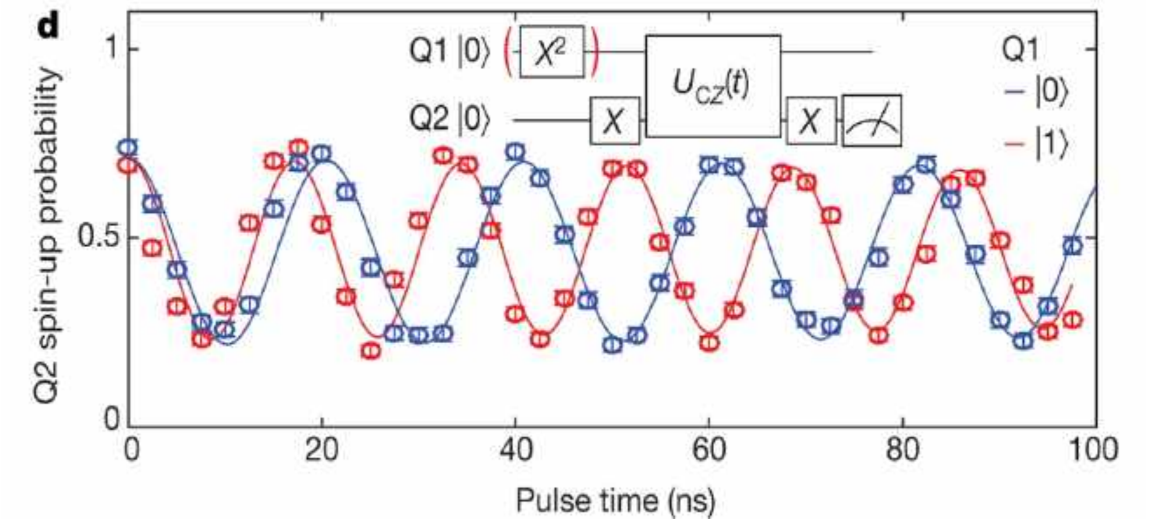
How to realize a two-qubit gate?

2-Qbit gate



Spin Exchange interaction





A Two-qubit quantum processor in silicon
Watson et al., Nature 2018 (TuDelft Si/SiGe)

Outlines

- Why silicon?
- Quantum toolbox for silicon qubit
- Perspectives for large scale

Toward a scalable platform

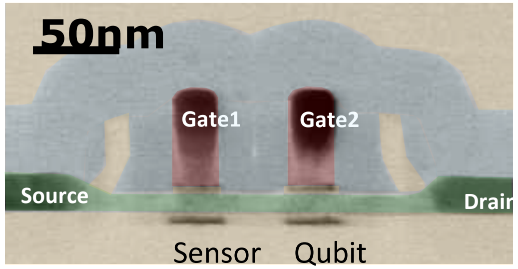
few qubits

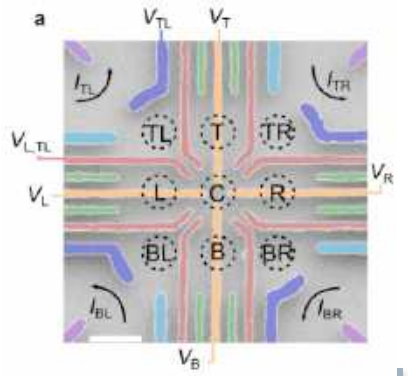
Challenges:

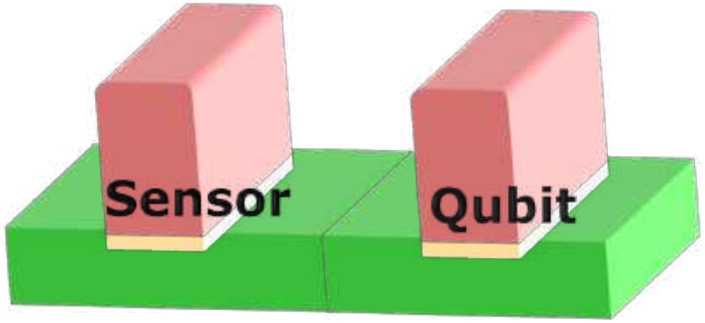
- Variability
- Integration and large-scale control

scalable (fault-tolerant) quantum processor

How to integrate sensors and qubits?







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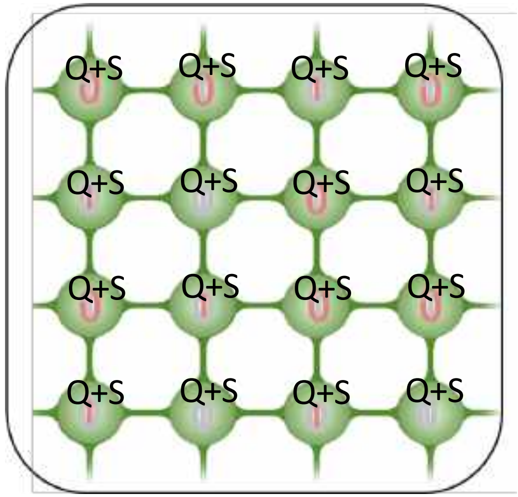

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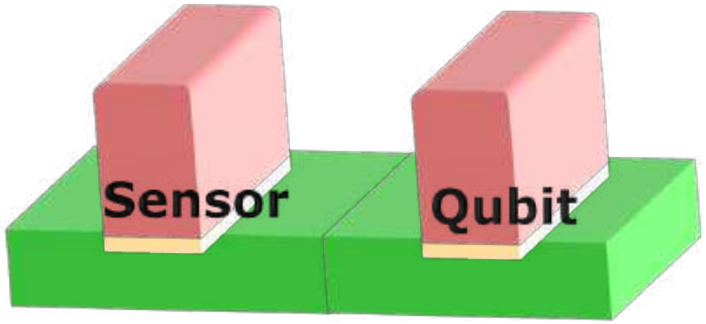
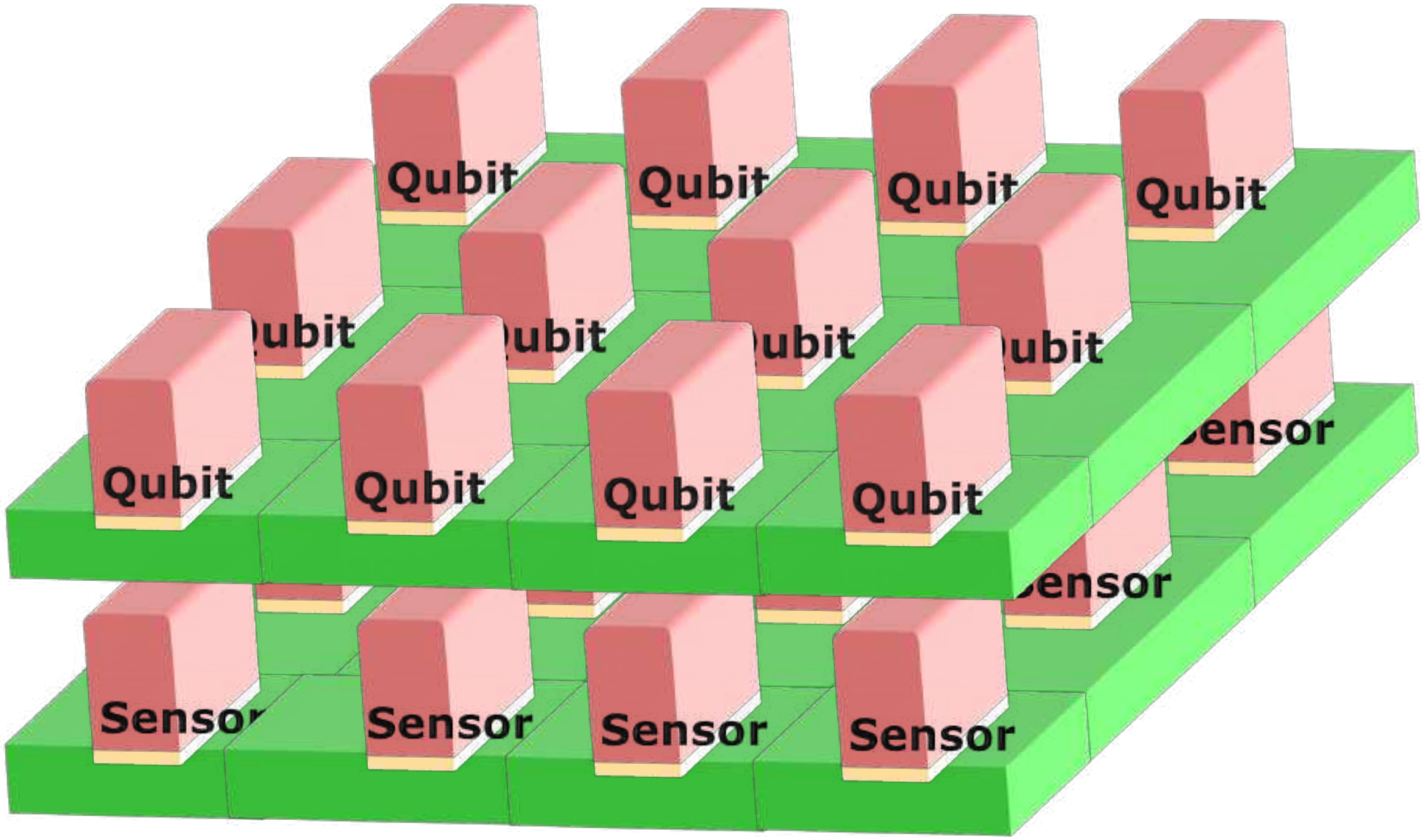
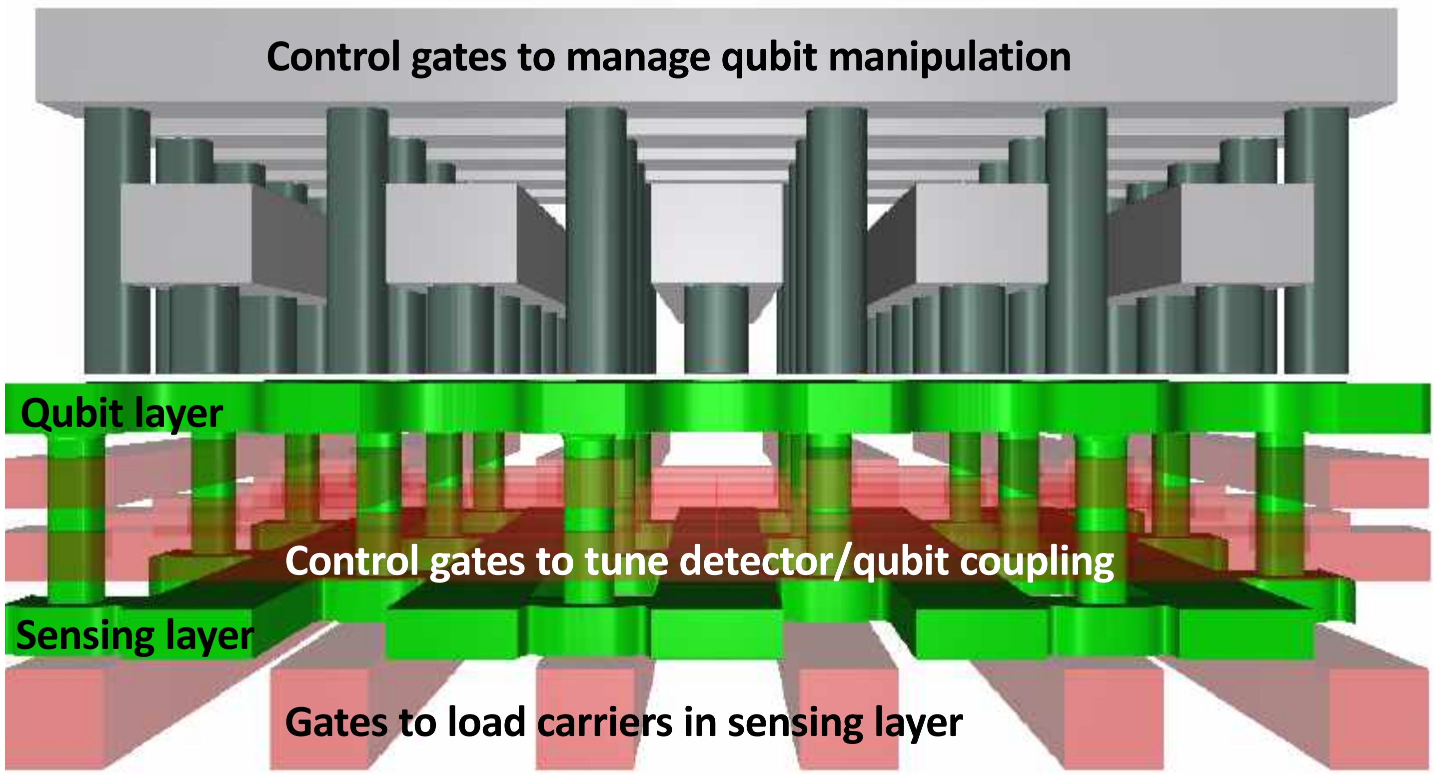


A 3D architecture



A 3D architecture

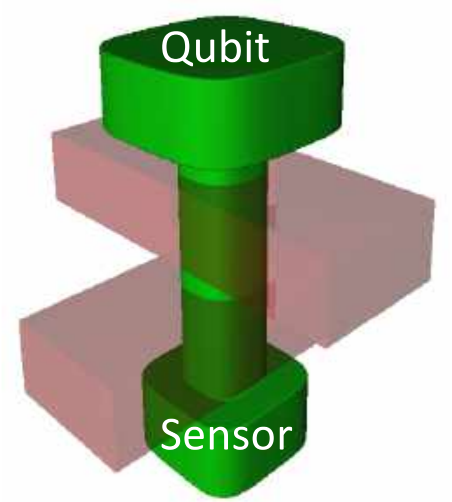
Patent *Meunier, De Franceschi, Vinet, Hutin (2017)*



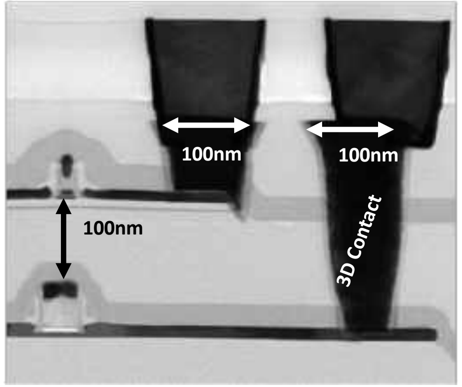
Technological challenge:

- Vertical tunneling for readout
- Muliplexing control and readout
- Quantum-classical interface

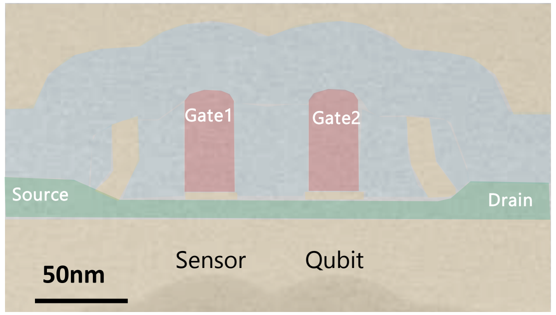
Challenge: vertical tunneling



Si *vias to interconnect the layers*



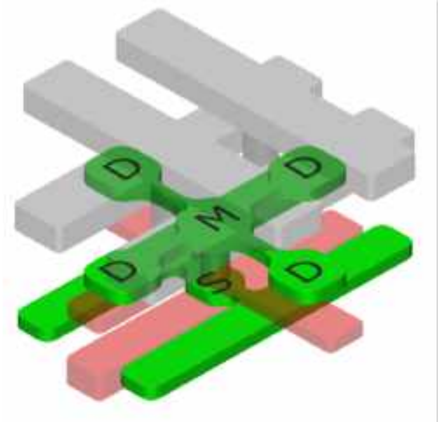
3D CMOS
Nanoscale integration
L. Brunet, VLSI (2017)
LETI

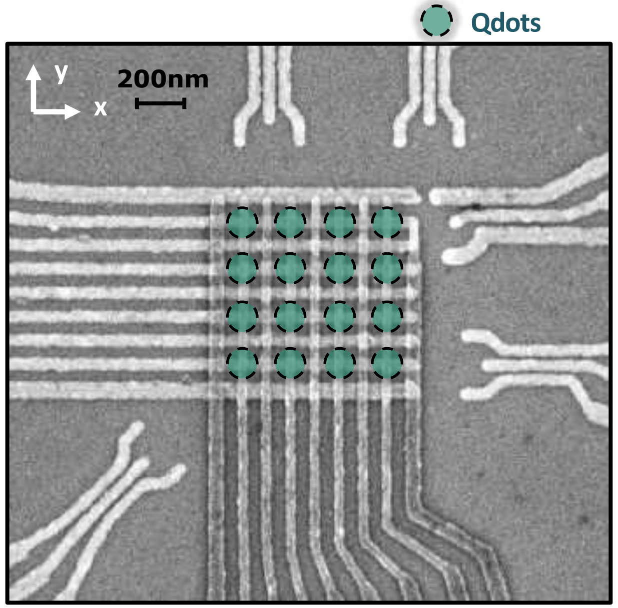


Lateral tunnel coupling
(experiment & simulation)
De Franceschi, IEDM (2016)

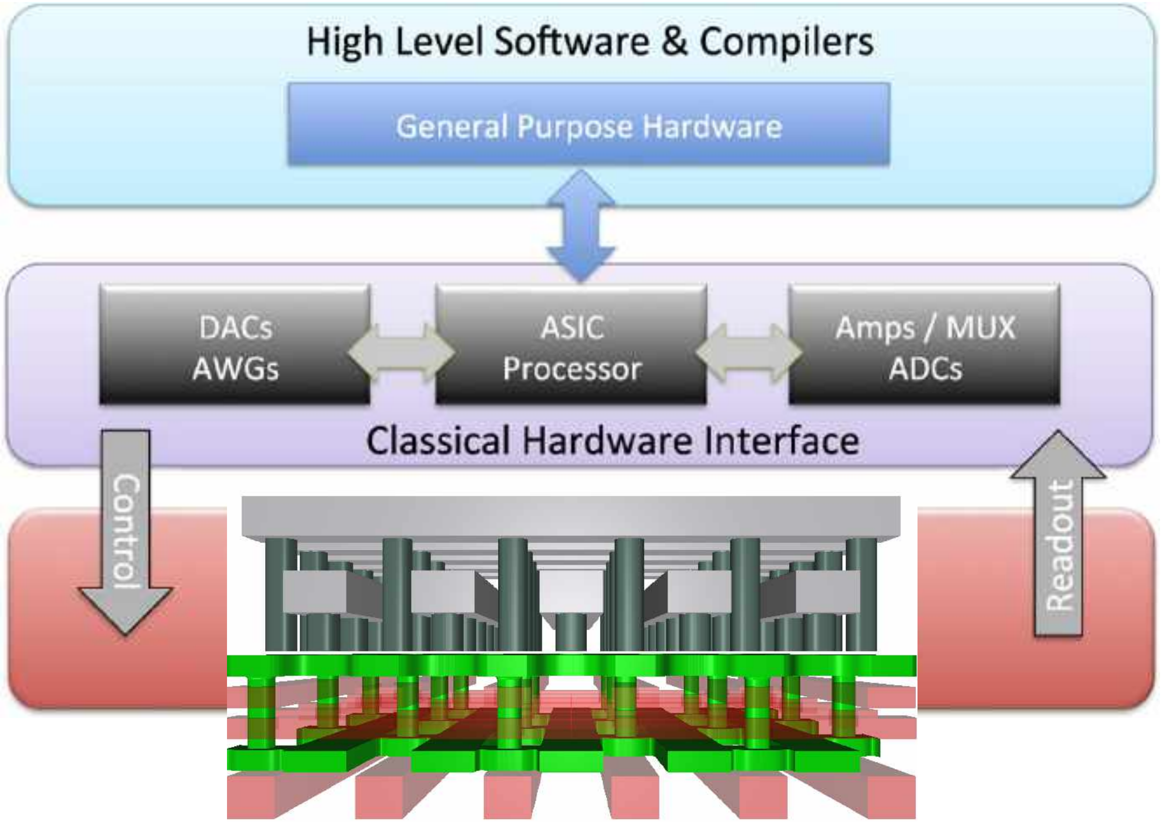
Challenge: line-column adressing

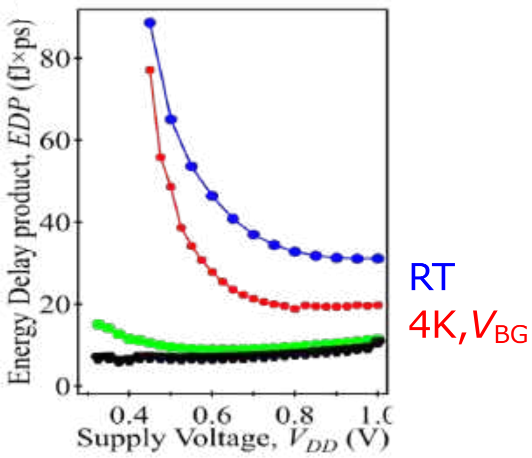
- Qubit layers + control layer
- For N^2 qubits: key points
  - o(N) controlled lines
  - Loading and read-out
  - 3D technology allow integrating all quantum functionalities in $(0.1\mu m)^3$
- For N^2 qubits: challenges
  - Variability
  - Operation selectivity





Challenge: cryo-electronic





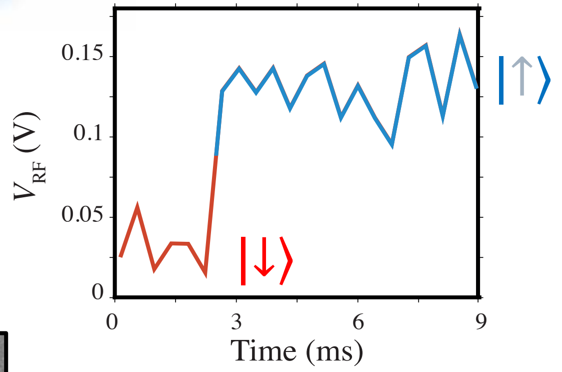
Exploiting cryo-CMOS

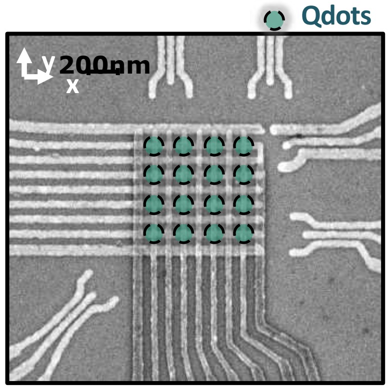
Bohuslavskyi et al, SNW (2017)

Reilly, NPJ Quantum Info(2015)

Conclusion

- Silicon is a promising platform for QC due to low decoherence and microelectronic potential
- We can fabricate readout and manipulate spin qubit in silicon
- Strong potential for large scale integration





Quantum Silicon Grenoble group

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