Towards Quantum Computing in Si MOS Technology: Single-shot Readout of Spin states in a FDSOI Split-Gate Device with Built-in Charge Detector

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Abstract

We report the first demonstration of real-time monitoring of a single spin in a Quantum Dot (QD) using foundry-compatible Si MOS technology and a Split-Gate design with built-in charge detector. Since single-shot readout is an indispensable step in the pursuit of Si-based fault-tolerant quantum computing, this work contributes to asserting the fabrication of Si spin qubits in a MOS technology platform as a viable and promising option.

Introduction

The building block of a quantum processor is the quantum bit (qubit) which is made out of a two-level quantum system. In contrast with a classical bit the information is encoded in a superposition of 0 and 1 (**Fig. 1**). Along with entanglement, this superposition of 0 and 1 (**Fig. 1**). Along with entanglement, this property can be harnessed by specifically designed algorithms to achieve a computational acceleration for applications such as cryptography, database search or simulation of quantum processes. In silicon-based quantum devices, the qubit is formed by the spin degree of freedom of a charge carrier (electron or hole) trapped in quantum dots. Tremendous progress has been achieved in this field in the past five years [1]. We recently demonstrated two-axis control of the first hole spin qubit in Si transistor-like structures using a CMOS technology platform [2,3]. In that proof-of-concept realization however, the qubit state was measured by averaging repeated destructive processes was measured by averaging repeated destructive processes followed each time by qubit re-initialization. In order to perform fault-tolerant quantum computation with dynamical error correction codes [4], single-shot (real-time) detection of the spin state is required [5]. This is achieved by a spin-to-charge conversion process in combination with a charge detection measurement, which requires coupling the qubit QD to local charge sensor Here we demonstrate this spin readout scheme in charge sensor. Here we demonstrate this spin readout scheme in a compact device consisting of a split-gate nEET realized using SOI nanowire technology on a 300-mm fab line.

Split-Gate devices and Quantum Dots

The fabrication flow and EM views on Fig. 2 describe the fabricated devices, which are nearly identical to conventional SOI Tabricated devices, which are hearly identical to conventional SOI NanoWire FETs. Following mesa patterning on 300mm undoped SOI wafers ($T_{Si}/T_{BOx}=12nm/145nm$), a high-k/MG stack was deposited and patterned using hybrid DUV/E-Beam lithography to achieve a 65nm Gate pitch. A particularly large spacer (30nm SiN) is defined prior to the self-aligned ion implants. Its primary purpose is to provide sufficient access resistance to localize charges in the Gate-defined QDs, hence enabling Single Electron Transietor (SET) operation A standard salicidation and Back-Transistor (SET) operation. A standard salicidation and Back-End-Of-Line process is then performed to complete the fabrication.

In the following, our device of interest has a "Split-Gate" geometry (W=45nm; $L_{G1}=L_{G2}=50$ nm; inter-Gate spacing S_{FF}=30nm) and n-type S/D doping. The electric field is strongest where the Gates wrap around the top mesa edges, hence defining "corner QDs" [6]. The spacer-protected thin undoped SOI regions on each side act as tunnel junctions providing longitudinal confinement. Each corner dot can be loaded with a small and tunable number of strongly confined electrons. With an adequate landscaping of the electrostatic potential in the channel, a third Single Electron Transistor (SET) can be formed in the a third Single Electron Transition (SET) can be formed in the middle of the mesa and between the Gates, with capacitive coupling to both QDs (**Fig. 3**). The DC transfer characteristic of this "built-in" SET – i.e. the gate-voltage position of its Coulomb peaks – is sensitive to any variation in the number of charges stored in either of the two corner QDs, as explained qualitatively in **Fig. 4**. It is thus essentially a charge detector.

Single-Shot Detection of a Quantum Dot Charge State

Fig. 5 shows a color scale mapping of I_{SET} vs. (V_{G1}, V_{G2}), measured at 350mK and for V_{DS} =150 μ V. A Coulomb peak is

materialized in this two-dimensional scan by a current ridge, and its ~45° angle indicates that the charge detector is equally coupled to V_{G1} and V_{G2} . In the following, we focus on detection on QD1. Indeed, a discontinuity is clearly visible at a given V_{G1}, which can be interpreted as the transition between two consecutive charge occupation numbers, M-1 and M, in QD1 [7]. A "read point" located on this boundary can be defined by choosing V_{G2} so that I_{SET} would be low if QD1 contained M-1 electrons, and high if it contained M electrons.

As the chemical potential of QD1 is aligned with the Fermilevel of an electron reservoir (e.g. Drain), the Mth electron may travel back and forth (**Fig. 6(a)**), causing the charge state of QD1 to fluctuate between M and M-1. This fluctuation can be tracked dynamically by monitoring I_{SET} toggling between two levels. Fig. **6(b)** shows the detection in real time of single charge events occurring every few ms (tunnel rate Γ_{OD1} : 400Hz – 1kHz).

Spin to Charge Conversion Using Energy-Selective Readout

As depicted in **Fig. 7**, when the QD contains an even number of M electrons, the Mth electron may occupy the same orbital as the M-1st if their spins are antiparallel. In case they have the same spin however, according to Pauli's exclusion principle, the Mth electron must occupy the next available orbital. As a consequence, there is an energy separation between these two spin configurations, corresponding to the orbital energy and the pairing energy. Hence, the charge state M in QD1 can be split in two levels noted $|G\rangle$ for "ground" and $|E\rangle$ for "excited", depending on the spin state of the (M-1; M) electron pair. V_{G1} can be adjusted so that the Drain Fermi-level lies between $|C\rangle$ and $|E\rangle$ This reaction to the split of the

 $|G\rangle$ and $|E\rangle$. This readout strategy is called "energy selective" [8], as tunneling of an electron to the Drain is allowed from $|E\rangle$ but it is forbidden from $|G\rangle$ due to lack of available states below the Fermi level of the reservoir. The principle is shown in Fig. 8, as well as corresponding measured I_{SET} time traces. Since the typical time for unloading an electron from QD1 into D was determined to be $T_{unload}=2.5$ ms, the readout measurement must be performed over a longer duration. This guarantees the appearance of a step-like signature when an electron in $|E\rangle$ leaves QD1, whereas I_{SET} remains high when $|G\rangle$ is occupied. This shows the successful remains high when $|G\rangle$ is occupied. This shows the successful conversion of spin information into a charge event detected by the central SET. As a sanity check, it can be useful to verify that the $|E\rangle$ spin state cannot relax to $|G\rangle$ within a measurement cycle. The protocol, illustrated in **Fig. 9**, consists in varying the latency time T_{wait} between loading an electron in QD1 and measuring I_{SET} in spin readout conditions. The probability of obtaining the "unloading" step response drops exponentially vs. T_{wait}, which means that after sufficiently long time QD1 is always in its ground state. A characteristic relaxation time T₁=13.5ms is extracted, which is consistent with typical values for electron pairs in Si [9,10].

Conclusion

We have shown an ultra-compact device fabricated in foundrycompatible Si MOS technology, with a built-in charge detector (SET) capacitively coupled to two Gate-defined QDs. Thanks to an energy-selective detection scheme, we have demonstrated single-shot readout of the spin-state in one of the QDs, which is an essential requirement to implement fault-tolerant quantum computing. As detailed in **Fig. 10**, further optimization of the readout speed/fidelity trade-off can be achieved by increasing the readout speed/indenty trade-on can be achieved by increasing the tunnel rates (*ie* decreasing the access resistance for both the QD_s and the SET) while keeping a large (Γ_{SET} - Γ_{QD}) window. On FDSOI, the possibility of using the back-Gate as an additional handle is an asset. In particular, it can be used to tune the cross-capacitance between the SET and the QD in order to improve the readout signal. Another longer-term advantage is the perspective of raducing the paragitics by seamlessly co-integrating Si qubits of reducing the parasitics by seamlessly co-integrating Si qubits with conventional control electronics circuitry.

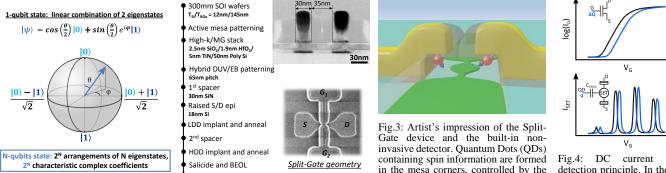


Fig.2: Left: simplified process flow. Top

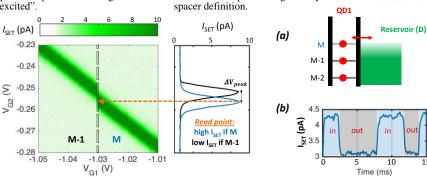
right: STEM view of two Gates in series

(65nm pitch) showing the width of the 1st

spacer. Bottom right: SEM top view of a

device with Split-Gate geometry after 1st

Fig.1: Bloch sphere representation of the quantum state space. A qubit state be described by a linear can combination of eigenstates *e.g.* "spin-up" and "spin-down" or "ground" and "excited".



1. Fill M

t probability 70 0.3 70 0.2

event_0.1

0

0

B = 0T T₁ = 13.5ms

 $|E\rangle$

 $|G\rangle$

Fig.5: Left panel: $I_{\rm SET}$ mapping vs. $V_{\rm G1}$ and $V_{\rm G2}$ the green trace materializes a Coulomb peak in the detector. On each side of the discontinuity (cf. dashed line), the position of the Coulomb peak vs. V_{G2} is shifted (by $\Delta V_{peak}=C_{CROSS}/q$) as the charge number in QD1 changes from M-1 to M. This is visible in the right panel, which also illustrates that fixing V_{G2} at an adequate read point (cf. orange arrow) enables discriminating the M-1 and M charge states in QD1, based on the value of I_{SET} (resp. low and high). Measurements were performed at $V_{\text{DS}}{=}150\mu\text{V}$ and T=350mK.

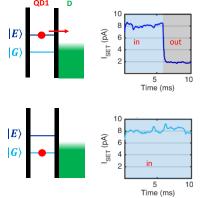


Fig.8: Spin to charge conversion scheme for single-shot readout. The Fermi energy of the reservoir is adjusted to lie between $|E\rangle$ and $|G\rangle$. In such a configuration, the Mth electron can only tunnel off the dot when in an excited spin state. The time domain response of I_{SET} performed over a duration longer than T_{unload} indicates whether tunneling has occured, thus giving information on the electron spin state.

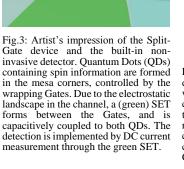
Fig.9: In order to extract the relaxation time T1, we first load an electron in the dot, wait for a varying time Twait and perform the spin measurement depicted in Fig.8. We repeat this measurement many times and plot the probability to detect an excited state is plotted vs. Twait. The probability tends towards 0 eventually, and the characteristic time $T_1 = 13.5$ ms is consistent with the expected spin relaxation times for electron pairs at zero magnetic field [10].

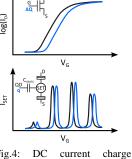
20

T_{wait} (ms)

2. Hold

meas $F(t) = A \cdot e^{-t/T_1} + c$





detection principle. In the same way that a $\Delta \hat{Q}$ in the Gate capacitance causes a shift of the transfer characteristics in a regular FET, an elementary charge variation in the QD coupled to the SET shifts the Coulomb peaks in the latter.

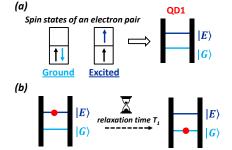


Fig.7: (a) The Pauli principle prevents two electrons with same spin from occupying the same orbital. Two configurations (Ground and Excited) are available for an even number M of electrons, and their energy difference corresponds to the orbital energy. Depending on its spin, the Mth electron can occupy the QD to yield either the $|G\rangle$ or $|E\rangle$ state. This can be leveraged in a spin detection scheme (cf. Fig. 8). (b) The spin state of the electron pair may spontaneously change from $|E\rangle$ to $|G\rangle$ after a

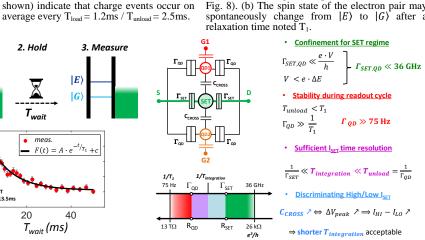


Fig.10: Schematic of the Split-Gate device. The central SET can remotely sense in real time a spin event occurring in the corner QDs. Ďesign windows in terms of Γ tunnel rates, and corresponding tunnel resistance (calculated at V=150µV) are represented, based on the right-hand side considerations. Increasing the red area yields a faster readout. Maximizing the SET-Dot cross-capacitance leads to improving the readout signal and thus enables to reduce the integration time, *i.e.* squeeze the blue area. Tuning C_{CROSS} however requires at least another adjustment handle, e.g. the Back-Gate on FDSOI.

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Fig.6: (a) If the chemical potential of M is

aligned with the Fermi level of a reservoir

(e.g. D), the charge state in QD1 may

fluctuate between M and M-1. (b) As a result, at the read point defined in Fig. 5, the SET

current switches in time domain between two

distinct levels when the electron leaves or re-

enters QD1. Statistical extractions (not

3. Measure

E

G

40

References: [1] M. Veldhorst et al., Nature 526, 410 (2015). [2] L. Hutin et al., VLSI (2016) [3] R. Maurand et al., Nat. Commun., 7, 13575 (2016) [4] A. G. Fowler, Phys. Rev. A 86, 032324 (2012) [5] A. Morello et al., Nature 467, 687 (2010) [6] S. De Franceschi et al., IEDM (2016) [7] L. M. K. Vandersypen et al., Appl. Phys. Lett. 85, 4394 (2004) [8] J. M. Elzerman et al., Nature, 430, 431 (2004) [9] M. Xiao et al., Phys. Rev. Lett., 104, 096801 (2010) [10] C. H. Yang et al., Nat. Commun. 4, 2069 (2013) Acknowledgment - The authors acknowledge financial support from the EU under Projects SiAM (No. 610637) and MOS-QUITO (No. 688539), the Marie Curie Fellowship within the Horizon 2020 program and the ANR-16-ACHN-0029.