Harnessing Si CMOS Technology for Quantum Information

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***Abstract* — We present some recent progress towards the implementation of the basic building blocks of quantum information processing derived from a Si CMOS technology platform. In our approach, characterized by an emphasis on foundry compatibility in terms of processes and materials, the so-called qubits are encoded in the spin degree of freedom of gate-confined elementary charges. After introducing various qubit manipulation, coupling and readout schemes, we discuss some prospects for scalability, and in particular some potential advantages of the FDSOI technology.**

I. Introduction

Among all solid-state implementations of quantum information processing, silicon-based qubits are particularly attractive in view of the possibility to leverage the well-established engineering and integration capabilities of microelectronics technology. This represents an asset in terms of upscaling potential, since fault-tolerant surface-code architectures are expected to include millions of physical qubits, individually addressed by classical circuitry for initialization, manipulation and readout [1]. Experimentally, Si-based spin qubits have been recently shown to feature very promising results in terms of quantum coherence and fidelity [2]. Meanwhile, the continued CMOS device scaling and pitch miniaturization tend to make these objects compatible with mass fabrication, thus making the development of spin qubits on an industry-standard CMOS platform a timely and viable opportunity.

II. Foundry-compatible Si spin qubits

Until recently, all Si-based qubits reported relied on either electron or nuclear spins. Single-qubit operations are performed by a local modulation of the effective magnetic field. In the case of holes, their inherently strong spin-orbit coupling offers the opportunity to perform single-qubit operations simply by a time-controlled microwave (MW) modulation of a gate voltage [3], thus eliminating the need for additional qubit-control elements (such as superconducting strips or micro-magnets). In order to demonstrate hole-spin qubit functionality we used a double quantum dot (QD) device based on SOI nanowire MOSFET technology [4] (Fig. 1). The device (Fig. 2) has an undoped silicon channel where two QDs are formed by hole accumulation under the two gates, coupled through a tunnel junction. Transport across the double QD is primarily dominated by the Coulomb blockade (CB) effect [5]. In addition, a spin blockade (SB) effect occurs when inter-dot tunneling requires antiparallel spins [6], as in the case of the $(1,1) \rightarrow (0,2)$ transition, where each digit represents the number of holes in each QD.

If the $|\uparrow\rangle$ and $|\downarrow\rangle$ states are splitted in QD1 by applying a static magnetic field (typically 0.1T), it is possible to induce a spin rotation by matching the frequency of an electric field MW excitation on G1 to that energy separation. The duration τ of the MW burst is used to control the spin rotation angle. Hence, the probability of lifting the SB oscillates with τ, which is verified by measuring the current across the device (Fig. 3). The oscillation amplitude decays with τ, reflecting spin dephasing. From Ramsey-fringes interference and Hahn-echo experiments [7] (not shown) we estimate an inhomogeneous dephasing time $T_2^* = 60$ ns, and an intrinsic coherence time $T_2 = 250$ ns. Although this is a first demonstration of an electrically-driven hole spin qubit in Si, tunable coupling and single-shot readout schemes, which are key requirements of quantum computers, have yet to be tackled. In the following, a different type of device geometry facilitating the demonstration of both is introduced.

III. Coupling and readout in split-gate devices

For intermediate channel widths and a wrapping gate geometry, it can be shown that two pronounced potential minima develop at the upper nanowire corners leading to a pair of clearly distinct QDs [8]. Splitting the single gate into two face-to-face gates enables independent electrostatic control of the two corner dots. The inter-dot coupling, mediated by tunneling and Coulomb interaction, can be further tuned by means of a back-gate voltage. In Fig. 4, we provide experimental evidence of this tunability. For $V_{BG} = -15$ V (Fig. 4.a)), the two dots are only weakly coupled. Current ridges with almost vertical (horizontal) slopes denote the addition of electrons to QD1 (QD2). For $V_{BG} = +30$ V (Fig. 4.b)), both dots are "pulled" toward the lower side of the channel and closer to each other. As a result, the current ridges associated with the first added electrons get remarkably tilted, denoting sizeable cross capacitances, and inter-dot capacitive coupling becomes noticeable.

In the presence of a small tunnel coupling ($t \sim 1$ μeV), one of the two QDs could be used to encode a qubit and the other one to perform readout, once again leveraging the SB effect, this time through RF gate reflectometry [9,10]. The readout setup is described in Fig. 5. An LC resonator, with resonance frequency in the few-hundred MHz range, is connected to the right gate, confining the readout QD. This connection contributes to a shift in the resonance frequency whose magnitude depends on the quantum capacitance associated with the spin-dependent inter-dot tunneling. Measuring the reflected RF signal gives information on this quantum capacitance and hence on the state of the spin qubit (in the left QD) relative to the reference readout spin (in the right QD), which remains always aligned to the external magnetic field. In principle, this technique can provide fast single-shot readout, and it is potentially scalable. The broadening of the split-gate device geometry to a Linear Nearest Neighbor (LNN) array (Fig. 6) would provide a useful starting ground for the implementation of a quantum error correction in a fault-tolerant logical qubit [11].

Another possible single-shot readout scheme consists in coupling a charge sensor (Quantum Point Contact or Single Electron Transistor) to a qubit-containing QD. In recent work [12], adequate landscaping of the electrostatic potential in a split-gate device (in particular, using the back-gate handle) led to the configuration shown in Fig. 7. An SET is coupled to each corner QD; its impedance can be probed *e.g.* by DC current measurement. A charge state transition in QD1 induces a Coulomb peak shift in the I_{SET}-V_{G2} characteristics, hence allowing direct detection of a single charge event. Spin-charge conversion is carried out via a so-called energy-selective scheme [13] explained on Fig. 8. If the Fermi energy of a reservoir electrode is made to lie between the spin-dependent "Ground" and "Excited" states of the M^{th} charge, the charge may only tunnel out of QD1 from the latter. Thus the time-domain signature of I_{SET}, constant or step-like, over a sufficiently large amount of time (depending on the QD1 tunnel rates) gives direct information on the qubit spin state.

IV. Prospects for scalability

The ability to tune cross-capacitance and tunnel rates between QDs, charge sensors, and leads is either essential or highly beneficial to performing two-qubit gate operations and single-shot readout, both of which are critical requirements for quantum computing. Yet, a trade-off arises between multiplying the optimization knobs and keeping the building blocks adequately compact for quantum circuits upscaling. Using Fully-Depleted SOI technology offers the possibility to use localized back-gates, thereby advantageously reducing cross-talk with the Dot-defining front-gates. A low aspect ratio of the top Si film and thin Buried Oxide are expected to provide enhanced sensitivity.

FDSOI CMOS technology typically features undoped channels, which is an asset for the reliable operation at very low temperatures of classical electronics needed to address each qubit. Besides, drastic power dissipation constraints also tend to impose a low supply voltage V_{dd}. It is possible to maintain or enhance the power-performance trade-off through a back-bias-mediated adjustment of the threshold voltage. In conclusion, FDSOI CMOS seems like a promising platform for large-scale co-integration of qubits and their peripheral control electronics.

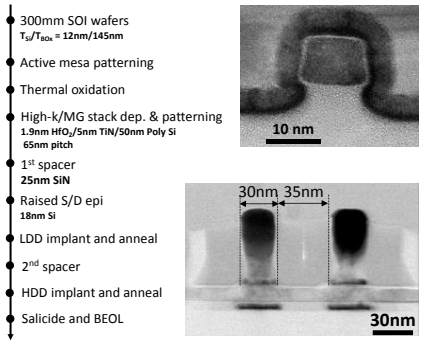

Fig. 1: Simplified process flow and TEM cross-sections along the Gate of an SOI NanoWire FET (top) and along the channels of two Gates in series (pitch 65nm). Wide spacers are primarily used for proper Gate-defined QD confinement, and to protect the inter-Gate spacing from self-aligned ion implantation.

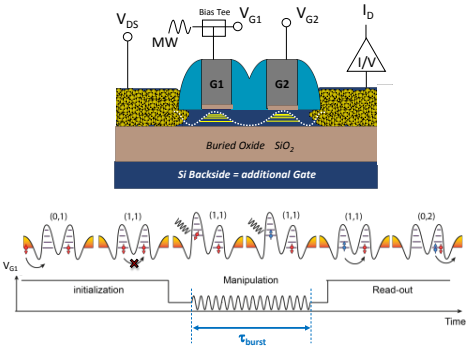

Fig. 2: (top) Cross-sectional sketch along the channel showing the Valence Band profile with the sub-spacer tunnel barriers and the quantization of states in the Gate-defined dots. The wiring scheme for qubit measurements is also shown. (bottom) Event sequence in a gate modulation period. Transport is blocked for the spin manipulation step. A microwave excitation on Gate 1 induces a coherent rotation of the spin in QD1. Transport is enabled again for readout.

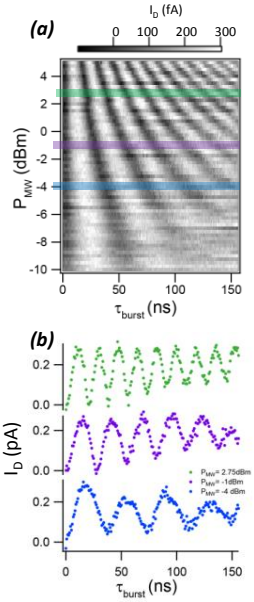

Fig. 3: a) Grey-scale plot of the device current, I_{sd}, as a function of MW burst duration, t_{burst}, and MW power, P_{MW}. Hole-spin coherent rotations are revealed by periodic oscillations of the current as a function of τ_{burst}. As expected, the Rabi rotation frequency increases linearly with $P_{MW}^{1/2}$. b) selected $I_{sd}(\tau_{burst})$ traces from a).

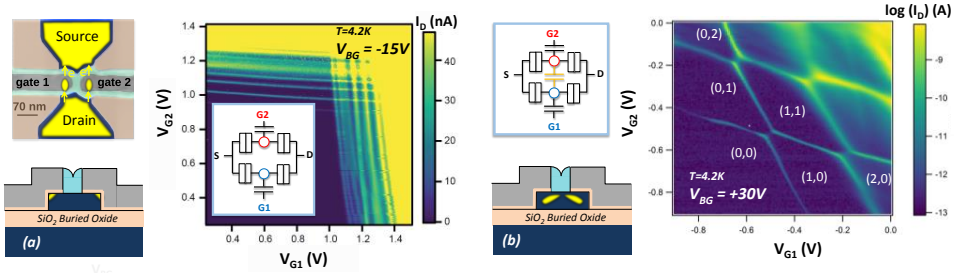

Fig. 4: (a) Drain current mapping measured in an n-type split-gate device at 4.2K against V_{G1} and V_{G2}, and for a negative V_{BG}= -15V. Each QD exhibits Coulomb peaks which are almost independent on the control voltage for the other QD. The dots are well separated, hence the mapping is a superposition of QD1's vertical and QD2's horizontal current ridges. (b) Mapping of log(I_D) in the same device, for a positive back-Gate bias V_{BG}= +30V. The current ridges are tilted, forming a honeycomb pattern delimiting the charge domains. This is a signature of capacitively coupled QDs.

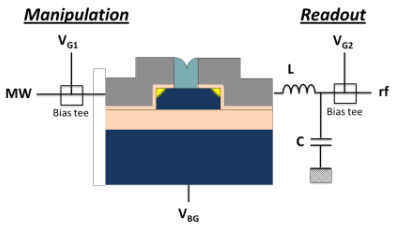

Fig. 5: Principle of the RF reflectometry measurement setup applied to a face-to-face device, enabling scalable, fast single-shot readout of the spin qubit state under G1.

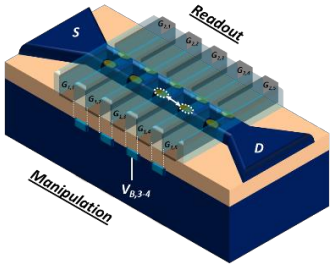

Fig. 6: One-Dimensional array of qubits along a Si NanoWire, using split-gate devices in series. Local Back-Gates formed in the Inter-dots spacings may provide selected tunability of nearest neighbor coupling.

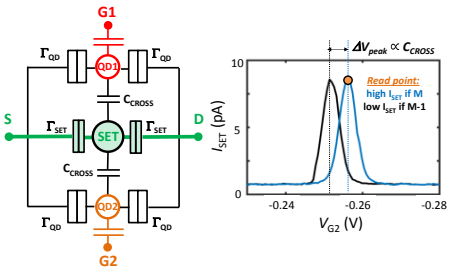

Fig. 7: (left) Schematic of a Split-Gate device with built-in charge detector. Tunnel rates are noted Γ. (right) The position of the Coulomb peak in the central SET vs. V_{G2} is shifted as the charge number in QD1 changes from M-1 to M. Fixing V_{G2} at an adequate read point enables discriminating M-1 and M in QD1, based on the value of I_{SET} (resp. low and high). Measurements were performed at V_{DS}=150μV and T=350mK.

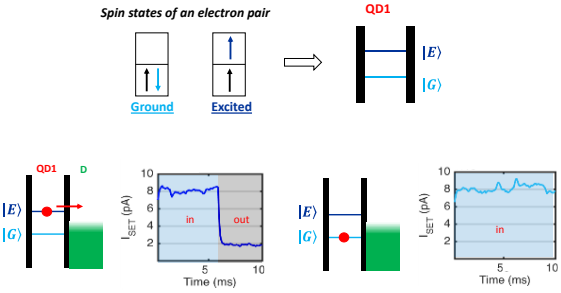

Fig. 8: Spin to charge conversion scheme for DC-SET single-shot readout. The Fermi energy of the reservoir is adjusted to lie between $|E\rangle$ and $|G\rangle$. In such a configuration, the M^{th} electron can only tunnel off the dot when in an excited spin state. The measured time domain response of I_{SET} performed over a duration longer than $T_{unload} = 1/\Gamma_{QD}$ indicates whether tunneling has occured, thus giving information on the electron spin state.

References: [1] A.G. Fowler *et al.*, Phys. Rev. A, 86, (2012). [2] M. Veldhorst *et al.*, Nature Nanotech., 9, (2014). [3] B. Voisin *et al.*, Nano Lett., 16, (2016). [4] L. Hutin *et al.*, VLSI Tech. Symp. 2016 [5] W.G. van der Wiel *et al.*, Reviews of Modern Physics, 75, (2002). [6] R. Hanson *et al.*, Reviews of Modern Physics, 79, (2007). [7] R. Maurand *et al.*, Nature Comm., 7, (2016). [8] B. Voisin *et al.*, Nano Lett., 14, (2014). [9] J. Colless *et al.*, Phys. Rev. Lett., 110, (2013). [10] A.C. Betz *et al.*, Nano Lett., 15, (2015). [11] C. Jones *et al.*, arXiv:1608.06335 [quant-ph]. [12] M. Urdampilleta *et al.*, VLSI Tech. Symp. 2017 [13] J. M. Elzerman *et al.*, Nature, 430, (2004).

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