SOI CMOS Technology for Quantum Information Processing

A path towards quantum bits and control electronics co-integration

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***Abstract*— We present some recent progress towards the implementation of semiconductor spin quantum bits derived from a Si CMOS technology platform. Our approach consists in developing a foundry-compatible embodiment of the basic building block of quantum information, with a strong potential for large scale co-integration of a quantum core with its mandatory classical control and readout electronics. After introducing various qubit manipulation, coupling and readout schemes, we discuss some prospects for scalability, and in particular some potential advantages of the FDSOI technology.**

Keywords—Silicon; CMOS; spin qubit; quantum computing; SOI

I. INTRODUCTION

A qubit is essentially a two-level quantum-mechanical system which, unlike a classical bit can be described by a superposition of its two basis states. Owing to the superposition and entanglement principles, an N-qubit state is characterized by 2^N complex coefficients corresponding to the normalized probabilities for each possible arrangement of basis states. This built-in parallelism in information treatment, if harnessed by proper algorithms [1], holds great promise for a variety of applications such as secure data exchange, database search, machine learning, and simulation of quantum processes. Among the various possible solid-state implementations satisfying the DiVincenzo criteria [2] for enabling quantum computation, silicon-based qubits are particularly attractive in view of the possibility to leverage the well-established engineering and integration capabilities of microelectronics technology. This represents an asset in terms of upscaling potential, since fault-tolerant surface-code architectures are expected to include millions of physical qubits, individually addressed by classical circuitry for initialization, manipulation and readout [3]. Experimentally, Si-based spin qubits have been recently shown to feature very promising results in terms of quantum coherence and fidelity [4]. Meanwhile, the continued CMOS device scaling and pitch miniaturization tend to make these objects compatible with mass fabrication, thus making the development of spin qubits on an industry-standard CMOS platform a timely and viable opportunity.

Furthermore, since each Si spin qubit i/ advantageously operates at sub-1K temperatures and ii/ needs to be addressed by classical electronics for manipulation and readout purposes, there has been a surge of interest for evaluating various technologies in terms of performance, noise and power dissipation trade-off [5], which in addition to other factors evoked in the following, underlines the interest of a SOI CMOS technology platform for quantum information processing and quantum computation.

II. FIRST CMOS-DERIVED SI HOLE SPIN QUBITS

Until recently, all Si-based qubits reported relied on either electron or nuclear spins. Single-qubit operations are performed by a local modulation of the effective magnetic field. In the case of holes, their inherently strong spin-orbit coupling offers the opportunity to perform single-qubit operations simply by a time-controlled microwave (MW) modulation of a gate voltage [6], thus eliminating the need for additional qubit-control elements (such as superconducting strips or micro-magnets). In order to demonstrate hole-spin qubit functionality we used a double quantum dot (QD) device based on SOI nanowire MOSFET technology [7] (Fig. 1).

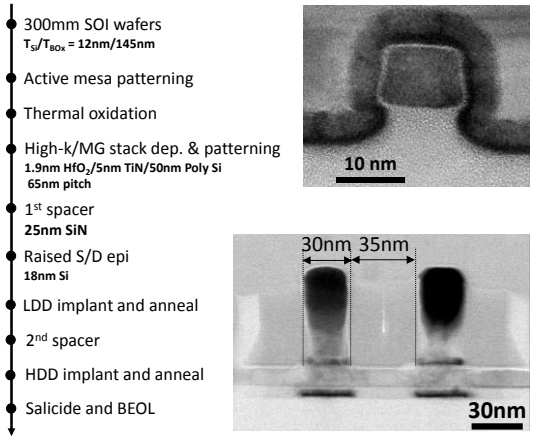


Fig. 1: Simplified process flow and TEM cross-sections along the Gate of an SOI NanoWire FET (top) and along the channels of two Gates in series (pitch 65nm). Wide spacers are primarily used for proper Gate-defined QD confinement, and to protect the inter-Gate spacing from self-aligned ion implantation.

The device represented schematically in Figure 2 features an undoped silicon channel where two QDs are formed by hole accumulation under the two gates, coupled through a tunnel

junction. At very low temperature, there is a quantization of the energy levels in each dot, and transport across the double QD is primarily dominated by the Coulomb blockade (CB) effect [8], which means that charges may transit one by one through the system. In addition, a so-called Pauli spin blockade (PSB) effect occurs when inter-dot tunneling requires antiparallel spins [9], as in the case of the (1,1) → (0,2) transition, where each digit represents the number of holes in each QD.

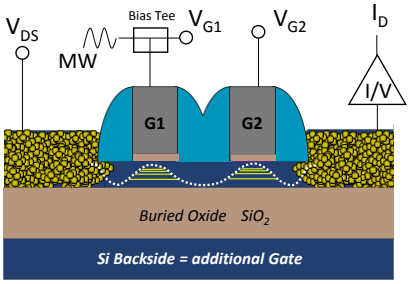


Fig. 2: Cross-sectional sketch along the channel showing the Valence Band profile with the sub-spacer tunnel barriers and the quantization of states in the Gate-defined dots. The wiring scheme for qubit measurements is also shown.

If the $|\uparrow\rangle$ and $|\downarrow\rangle$ states are splitted by applying a static magnetic field (typically 0.1T), it is possible to induce a spin rotation in QD1 by matching the frequency of an electric field MW excitation on G1 to that energy separation. The duration τ of the MW burst is used to control the spin rotation angle. Hence, the probability of lifting the PSB oscillates with τ, which is verified by measuring the current across the device (Fig. 3).

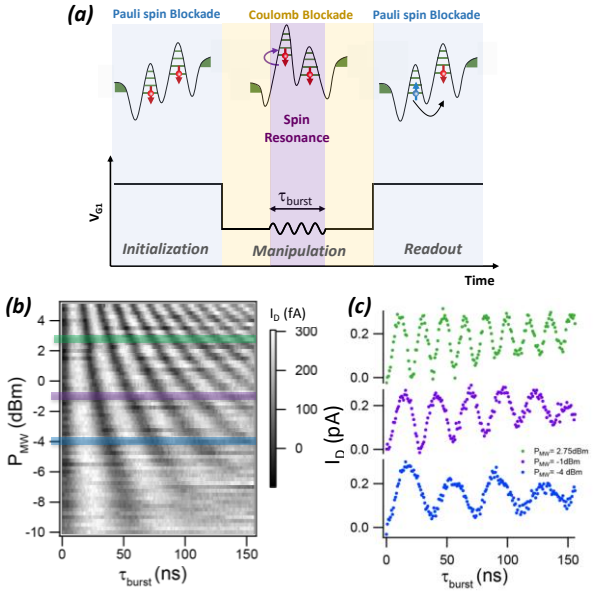


Fig. 3: (a) Event sequence in a gate modulation period. Transport is blocked for the spin manipulation step. A microwave excitation on Gate 1 induces a coherent rotation of the spin in QD1. Transport is enabled again for readout. (b) Grey-scale plot of the device current, I_{sd}, as a function of MW burst duration, t_{burst}, and MW power, P_{MW}. Hole-spin coherent rotations are revealed by periodic oscillations of the current as a function of τ_{burst}. As expected, the Rabi rotation frequency increases linearly with $P_{MW}^{1/2}$. (c) selected $I_{sd}(\tau_{burst})$ traces from (b).

The oscillation amplitude decays with τ, reflecting spin dephasing. From Ramsey-fringes interference and Hahn-echo experiments [10] (not shown) we estimate an inhomogeneous dephasing time $T_2^* = 60$ ns, and an intrinsic coherence time $T_2 = 250$ ns. Although this experiment is a first demonstration of an electrically-driven hole spin qubit in Si, it does not show tunable coupling and single-shot readout schemes, which are key requirements for quantum computing. In the following, a different type of device geometry facilitating the demonstration of both is introduced.

III. Coupling and Readout in Split-Gate Devices

For intermediate channel widths and a wrapping gate geometry, it can be shown that two pronounced potential minima develop at the upper nanowire corners leading to a pair of clearly distinct QDs [11]. Splitting the single gate over the channel into two face-to-face gates enables independent electrostatic control of the two corner dots. The inter-dot coupling, mediated by tunneling and Coulomb interaction, can be further tuned by means of a back-gate voltage. In Fig. 4, we provide experimental evidence of this tunability. For $V_{BG} = -15$ V (Fig. 4.a)), the two dots are only weakly coupled. Current ridges with almost vertical (horizontal) slopes denote the addition of electrons to QD1 (QD2). For $V_{BG} = +30$ V (Fig. 4.b)), both dots are "pulled" toward the lower side of the channel and closer to each other. As a result, the current ridges associated with the first added electrons get remarkably tilted, denoting significant cross capacitances, and inter-dot capacitive coupling becomes noticeable.

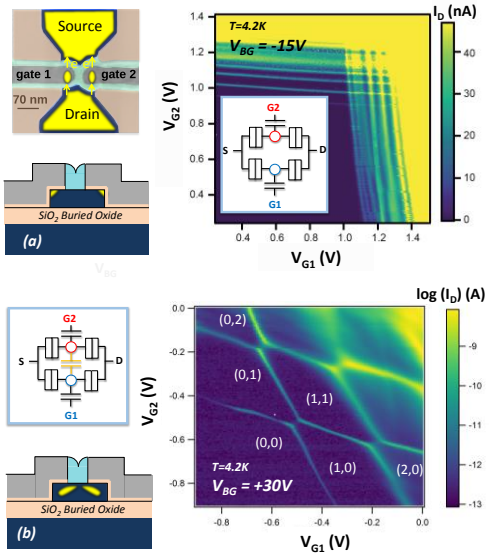


Fig. 4: (a) Drain current mapping measured in an n-type split-gate device at 4.2K against V_{G1} and V_{G2}, and for a negative V_{BG}= -15V. Each QD exhibits Coulomb peaks which are almost independent on the control voltage for the other QD. The dots are well separated, hence the mapping is a superposition of QD1's vertical and QD2's horizontal current ridges. (b) Mapping of log(I_D) in the same device, for a positive back-Gate bias V_{BG}= +30V. The current ridges are tilted, forming a honeycomb pattern delimiting the charge domains. This is a signature of capacitively coupled QDs.

In the presence of tunnel coupling (t ~ 1 µeV), one of the two QDs could be used to encode a qubit and the other one to perform readout, once again leveraging the PSB effect, this time through RF reflectometry [12,13]. The readout setup is described in Fig. 5. An LC resonator, with resonance frequency in the few-hundred MHz range, is connected to the right gate, confining the readout QD. This connection contributes to a shift in the resonance frequency whose magnitude depends on the quantum capacitance associated with the spin-dependent inter-dot tunneling. Measuring the reflected RF signal gives information on this quantum capacitance and hence on the state of the spin qubit (in the left QD) relative to the reference readout spin (in the right QD), which remains always aligned to the external magnetic field. In principle, this technique can provide fast single-shot readout, and it is potentially scalable. The broadening of the split-gate device geometry to a Linear Nearest Neighbor (LNN) array (Fig. 5) would provide a useful starting ground for the implementation of a quantum error correction in a fault-tolerant logical qubit [14].

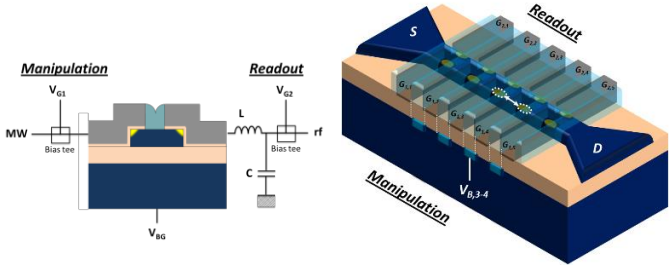


Fig. 5: (a) Principle of the RF reflectometry measurement setup applied to a face-to-face device, enabling scalable, fast single-shot readout of the spin qubit state under G1. (b) One-Dimensional array of qubits along a Si NanoWire, using split-gate devices in series. Local Back-Gates formed in the Inter-dots spacings may provide selected tunability of nearest neighbor coupling.

Another possible single-shot readout scheme consists in coupling a charge sensor (Quantum Point Contact or Single Electron Transistor) to a qubit-containing QD. In recent work [15], adequate landscaping of the electrostatic potential in a split-gate device (in particular, using the back-gate handle) has led to the configuration shown schematically in Fig. 6.

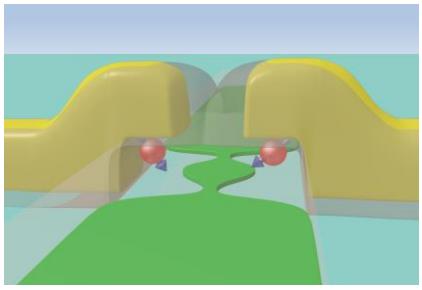


Fig. 6: Artist's impression of the Split-Gate device and the built-in non-invasive detector. Quantum Dots (QDs) containing spin information are formed in the mesa corners, controlled by the wrapping Gates. Due to the electrostatic landscape in the channel, a Single Electron Transistor with lateral constrictions (schematically materialized by the green boundaries) forms between the Gates, and is capacitively coupled to both QDs.

An SET is coupled to each corner QD; its impedance can be probed *e.g.* by DC current measurement. A charge state transition in QD1 induces a Coulomb peak shift in the I_{SET}-V_{G2} characteristics, hence allowing direct detection of a single charge event. The principle of detection is shown on Figure 7 and operates in the same way that a Back-Gate bias would induce a threshold voltage shift in a SOI MOSFET. Ideally, the Coulomb peaks should be well separated in order to maximize the ($I_{HI} - I_{LO}$) resolution at the read point. ΔV_{peak} is proportional to the cross-capacitance C_{CROSS} between the probed QD and the detector [8].

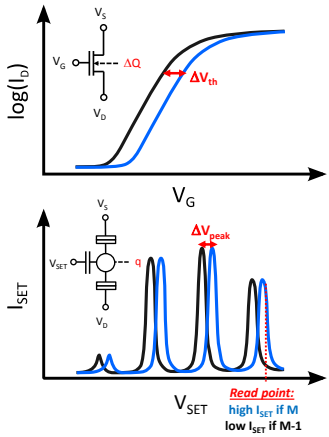


Fig. 7: DC current charge detection principle. In the same way that a ΔQ coupled to the channel causes a shift of the transfer characteristics in a regular FET, an elementary charge variation in the vicinity of the SET, for example in a capacitively coupled QD, shifts the Coulomb peaks in the latter.

Detecting a charge event in real time is then possible by probing I_{SET} over a duration larger than the time it takes for a charge to exit or enter QD1. This time depends on the characteristic tunnel rates Γ_{QD} of the junctions on either side of the QD, $T_{unload} = 1/\Gamma_{QD}$. A spin-charge conversion strategy is then necessary to turn this process into a spin readout mechanism. This can be carried out via a so-called energy-selective scheme [16] explained on Fig. 8. If the Fermi energy of a reservoir electrode is made to lie between the spin-dependent "Ground" and "Excited" states of the M^{th} charge, the charge may only tunnel out of QD1 from the latter. Thus the time-domain signature of I_{SET}, constant or step-like, over a sufficiently large amount of time gives direct information on the qubit spin state. In the case of [15], the Ground and Excited states are defined as the singlet and triplet configuration of the last two M and M-1 electrons of a total number M=2n in QD1. There is a relaxation time noted T_1 beyond which the Excited state relaxes to Ground. It is therefore crucial that this time should be larger than T_{unload}, which sets a lower bound for measurement time.

Fig. 9 synthesizes some design guidelines for optimizing the readout time in a more general case for which an SET is coupled to a single Quantum Dot. Fast readout is achieved by setting Γ_{QD} as large as possible. This increase is yet constrained by the fact that a large Γ_{SET}-Γ_{QD} window should remain to preserve a good readout fidelity. Having the ability to increase the cross-capacitance C_{CROSS} enables to improve the measurement resolution, or alternatively to perform a faster readout with no penalty on the fidelity.

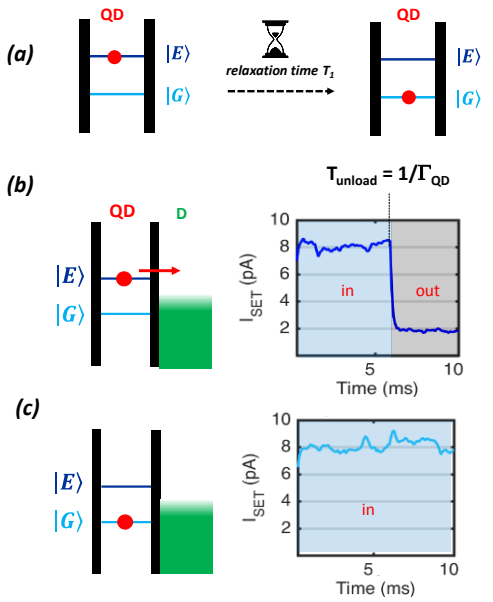
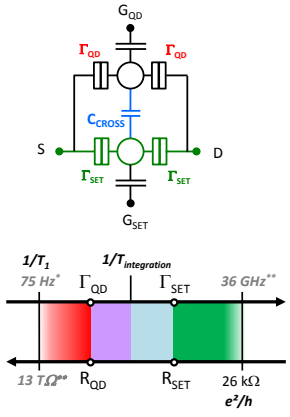


Fig. 8: Schematic view of the excited $|E\rangle$ and ground $|G\rangle$ spin states of an electron pair. The spin state may spontaneously change from $|E\rangle$ to $|G\rangle$ after a relaxation time noted T_1. (b) and (c) Spin to charge conversion scheme for single-shot readout. The Fermi energy of the reservoir is adjusted to lie between $|E\rangle$ and $|G\rangle$. In such a configuration, the M^{th} electron can only tunnel off the dot when in an excited spin state. The time domain response of I_{SET} performed over a duration longer than $T_{unload} = 1/\Gamma_{QD}$ indicates whether tunneling has occured, thus giving information on the electron spin state.



- **Confinement for SET regime**

$$\left.\begin{array}{l}\Gamma_{SET,QD} \ll \dfrac{e \cdot V}{h} \\ V < e \cdot \Delta E\end{array}\right\} \; \Gamma_{SET,QD} \ll 36\ \text{GHz}$$

- **Stability during readout cycle**

$$T_{unload} < T_1$$
$$\Gamma_{QD} \gg \frac{1}{T_1} \qquad \Gamma_{QD} \gg 75\ \text{Hz}$$

- **Sufficient I_{SET} time resolution**

$$\frac{1}{\Gamma_{SET}} \ll T_{integration} \ll T_{unload} = \frac{1}{\Gamma_{QD}}$$

- **Discriminating High/Low I_{SET}**

$$C_{CROSS} \nearrow \Leftrightarrow \Delta V_{peak} \nearrow \Rightarrow I_{HI} - I_{LO} \nearrow$$

$\Rightarrow$ shorter $T_{integration}$ acceptable

Fig. 9: Design windows in terms of Γ tunnel rates, and corresponding tunnel resistance (calculated at V=150μV) are represented, based on the right-hand side considerations. Increasing the red area yields a faster readout. Maximizing the SET-Dot cross-capacitance leads to improving the readout signal and thus enables to reduce the integration time, *i.e.* squeeze the blue area. Tuning C_{CROSS} however requires at least another adjustment handle, *e.g.* the Back-Gate on FDSOI.

IV. Prospects for Scalability

The ability to tune cross-capacitance and tunnel rates between QDs, charge sensors, and leads is either essential or highly beneficial to performing two-qubit gate operations and single-shot readout, both of which are critical requirements for quantum computing. Yet, a trade-off arises between multiplying the optimization knobs and keeping the building blocks adequately compact for quantum circuits upscaling. Using Fully-Depleted SOI technology offers the possibility to use localized back-gates, thereby advantageously reducing cross-talk with the Dot-defining front-gates. A low aspect ratio of the top Si film and thin Buried Oxide are expected to provide enhanced sensitivity.

FDSOI CMOS technology typically features undoped channels, which is an asset for the reliable operation at very low temperatures of classical electronics needed to address each qubit. Besides, drastic power dissipation constraints also tend to impose a low supply voltage V_{dd}. It is possible to maintain or enhance the power-performance trade-off through a back-bias-mediated adjustment of the threshold voltage. In conclusion, FDSOI CMOS seems like a promising platform for large-scale co-integration of qubits and their peripheral control and readout electronics.

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