NOVEL FABRICATION TECHNIQUE FOR SINGLE ELECTRON DEVICES

V. Bouchiat, D. Vion, D. Esteve and M. H. Devoret
Service de physique de l'état condensé
CEA-Saclay, 91191 Gif-sur-Yvette, France

Abstract

We present a new method for fabricating multilayer single-electronic circuits with vias, crossings and reduced cross-capacitances. A single electron transistor (SET) was fabricated with this method and successfully operated. Its intrinsic charge noise, 3×10^{-4} e/$\sqrt{\text{Hz}}$ at 10 Hz, matches that of other SETs.

Introduction

When single electron devices are fabricated using a single lithography step, the electrostatic coupling takes place through coplanar capacitors which are weak, subject to cross-talk and not compatible with a general network topology. These drawbacks have motivated the fabrication of multilayered circuits with overlapping capacitors [1]. Moreover, implementing with only two conductive layers all the features of a three dimensional network (composed of tunnel junctions and capacitances), necessitates an insulating spacer pierced in some points for connections (i.e. vias).

We present here a method for fabricating single electronic devices enabling crossings and vias. In our process, insulating layers are made of polyimide films.

Fabrication

In the first step, we perform an optical lithography of the connecting circuitry and of the gate electrodes. In our case, we evaporate 50nm of gold onto an oxidized silicon wafer.

In a second step, we spin a polyimide resist over the sample. Its final thickness after a 1 hour vacuum hardbake at 350°C is 0.4μm. We then open by reactive ion etching 1μm^2 large windows through the resist, thus uncovering the connecting leads. The etching parameters are chosen in order to obtain smooth enough window edges thereby enabling electrical continuity when the upper layer is evaporated.

The third step is a standard (MAA/PMMA bilayer) electron-beam lithography of the tunnel junctions defining the core of the device. This step requires an alignment with 0.1μm accuracy before exposure to ensure a correct positioning of the contacts and of the islands between junctions with respect to the windows and the buried gates. Finally, 0.1×0.1μm^2 Al/AlO_x/Al tunnel junctions are fabricated by evaporation at two angles through a shadow mask (see Fig. 1).

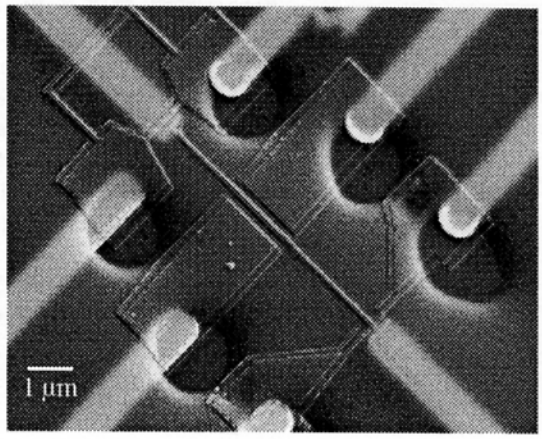

Figure 1: Scanning electron micrograph of a typical sample. The bright fingers are gold leads and gates under the polyimide film. Windows through the polyimide appear as circular black holes. Junctions and parts of the island lie over the two gates. The device consists of an electrometer (bottom right) which measures by its long thin strip shaped island the charge of an electron box (upper left).

Noise characterization

We have tested our process by fabricating and operating a single electron transistor (Fig. 1). This device is known to be the most sensitive electrometer [2] (see Fig. 2). Any variation in the electrostatic field near the island of the electrometer due to the motion of charges in the lower layers [3,4], induces a polarization charge q_n, the so-called charge noise of the electrometer. The noise q_n determines the detection limit of the electrometer. Therefore, a question about our new device arises : Is an organic film such as the polyimide a sufficiently "quiet" substrate for single electronics ?

To answer this question, we have measured the noise power spectrum of the electrometer designed to measure the charge in an electron box. Noise measurements were made in a dilution refrigerator at 20mK at a constant current bias I_b maximiz-

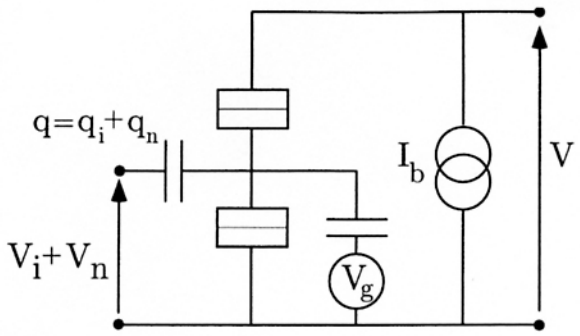

Figure 2: Schematic diagram of a SET electrometer. For a given gate voltage V_g, the output voltage V is a periodic function of the input charge q_i. The sensitivity $\partial V/\partial q$ depends on both V_g and the current bias I_b. The detection limit is determined by the superimposed input charge noise q_n.

ing the sensitivity $\partial V/\partial q$ of the electrometer. Each line connecting the device to the apparatus at room temperature was carefully filtered using miniature cryogenic filters [5]. Since we wanted to characterize the low frequency part of the noise we had to reject the 1/f noise generated by the amplifiers. Using a lock-in technique, the charge noise was shifted to higher frequencies at which the amplifier noise is orders of magnitude lower.

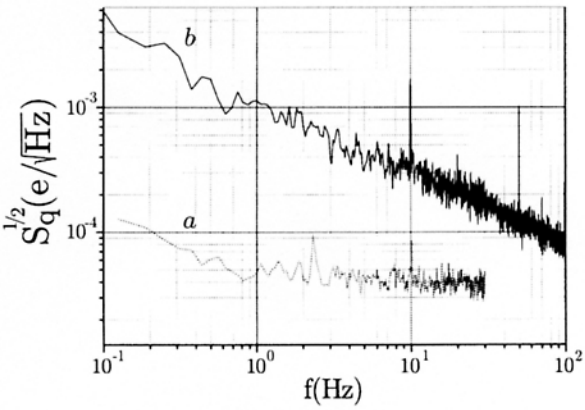

Figure 3: Noise spectral densities of the SET electrometer. a) noise at zero sensitivity : it includes noise of the whole setup. b) Charge noise at maximum sensitivity.

The charge noise power spectrum S_q shown on Fig. 3 displays a 1/f dependence. This is in agreement with the fact that the noise is generated by a collection of charge traps in the substrate, each trap emitting a telegraphic noise with distributed switching times [6].

The noise level at 10Hz is equal to $3\times10^{-4}e/\sqrt{\text{Hz}}$. Despite the large area of the electrometer island ($10 \times 0.1\mu m^2$), this value is of the same order of magnitude as those currently reported for electrometers fabricated on various kinds of inorganic substrates.

In conclusion, we have developed a new method for fabricating multilayer single electron devices enabling full 3D features without increasing the noise level. It enables the fabrication of more complex circuits such as Cooper pair pump arrays.

References

[1] E.H. Visscher, S. M. Verbrugh, J. Lindeman, P. Hadley, and J. E. Mooij. Appl. Phys. Lett., Vol. 66, p. 305, 1995.

[2] T. A. Fulton, and G.J. Dolan Phys. Rev. Lett., Vol. 59, p. 109, 1987.

[3] A.B. Zorin, F.J. Ahlers, J. Niemeyer, T. Weinmann, and H. Wolf. to be published, 1995.

[4]S.M. Verbrugh, M. L. Benhamadi, E. H. Visscher, and J. E. Mooij J. Appl. Phys., Vol. 78, p. 2830, 1995.

[5] D.Vion, P. F. Orfila, P. Joyez, D. Esteve, and M. H. Devoret. J. Appl. Phys., Vol. 77, p. 2519, 1994.

[6] C. T. Rogers, R. A. Buhrman, W.J. Gallagher, S. T. Raider, A.W. Kleinsasser, and R. L. Sandstrom. IEEE Trans. Magn., Vol. 23, p. 1658, 1987.