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Random Telegraph Signal and conduction properties of SOI deca-nano-Silicon Wires

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Abstract

A very small Silicon channel ("deca-nano-wire") was fabricated and its electric conduction properties were studied at room and cryogenic (4K) temperature. A strong non linearity was observed in the electric conduction at 4K, whereas a much more plain resistive behaviour was found when temperature was raised above 150K. The Gate voltage dependence of the conductance evidenced complex (yet definitely reproducible) features suggesting a complex potential distribution along the doped silicon channel. We believe that the conduction along the channel is of a percolative type, however, it proves difficult to conclude between a Coulomb blockade dominance and variable range hopping conduction. A more conclusive single electron behaviour was detected by the mean of time statistics of the flowing current, since a very strong amplitude random telegraph signal was measured.

Introduction

Within the general shrinking trend of VLSI microelectronics, it appears of strong importance to study and understand the physics of electrical conduction of ultimately small silicon channel. Small silicon wires have already been studied [1] and in some cases Coulomb Blockade (CB) was reported at cryogenics temperatures. To our knowledge, the precise origin of this phenomenon is however still not clearly understood. Some authors invoke the geometrical non-uniformity of the width of the wire, others suggest that a dopant distribution is at the origin of this phenomenon [2]. We will try here to bring new hints into this field. In particular, we investigate statistics on the current time evolution in a stationary voltage potential configuration.

Device Fabrication

Silicon wires of 15nm thick, 40-100nm wide and approx. 2µm long were fabricated with an extrapolation of a fully depleted SOI .25µm technology (8'' Smartcut®). Thinning was achieved by Local Oxidation of Silicon (LOCOS) and contact areas 80nm were defined to preserve further W/TiN/Ti contacts. A two step doping was necessary in order to obtain degeneracy in contact areas without damaging thinner wire region. Wires were doped with As 5e13cm-2 8keV. A 200nm Poly Silicon (doped in situ) Gate was added after 7-20nm High Thermal Oxide deposition. A conventional USG/PSG oxide deposition and AlCu metallisation terminated the process. For cryogenics measurements, dices were mounted on ceramic packaging with Al wires.

Electrical Results

Electrical current was measured with Lock in Amplifier at 500Hz. The I_{SD}-V_{SD} curve shows a strong non linearity at 4K (**fig1**), which vanishes above 150K leaving a mostly resistive behaviour. The current gate voltage dependence (**fig2**) reveals complex features that can hardly be interpreted by a pure (few dots) coulomb blockade behaviour. To our point of view, these current oscillations rather evidence a complex potential distribution within the wire, implying erratic yet reproducible percolative charge transport. The resistivity of the wires increases strongly when the width shrinks from 100nm to 40nm (f**ig3**). We infer that this is due to the fewer percolative paths available in the wire when size reduces to only a few electron wave packet size. The Time evolution statistics (**fig4**) reveals clear Random Telegraph Signals. The most common feature was multilevel RTS yet some fine tuning of the voltages applied was necessary in order to evidence a 2-level RTS. The temperature evolution (**fig5**) of the average τh (top level lifetime) and τb (bottom level lifetime) are in good accordance with thermal activation of a bistable physical system. Similar phenomenon have been observed on MOSFET channel current: trapping/detrapping of a charge in a defect at the Si/SiO2 interface [3]. In that case however, the current variation amplitude between 2 levels is roughly the ratio of the single charge trapped to the total number of charges in the channel. Here, this ratio is much greater. Moreover, the V_G and V_D evolution (**fig6&7**) of τh and τb, are here non monotonous. This can hardly be understood by a Field Effect on the channel due to a trapping/detrapping taking place at the Si/SiO2 interface. On the other hand, such a behaviour is not surprising if one imagines that the displacement of a single charge within the wire can deeply affect the percolation paths available within the wire.

Conclusion

Low temperature Electrical study of the deca-nano-wires revealed several mono-electronic transport features : a non linear Id-Vd curve, a complex Id-Vg behaviour and a Random Telegraph Signal of Id. These data suggest a percolative type conduction within the wire. New devices that should give more detailed insight into the physics involved are presently under process.

Acknowledgments

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References

[1] H.O Müller. Mat. Science & Eng. B74(2000) 36; R.Smith Alexandria 1996 A-3.118; V.Ng J. Appl. Phys. 86-12(1999) 6931.
[2]T.Koester Jpn.J.Appl.Phys.38(1999) 465.
[3] G.Ghibaudo, Microelec. Eng. 39(1997) 31; A.Ohata J.Appl.Phys. 38(1999) 2473.

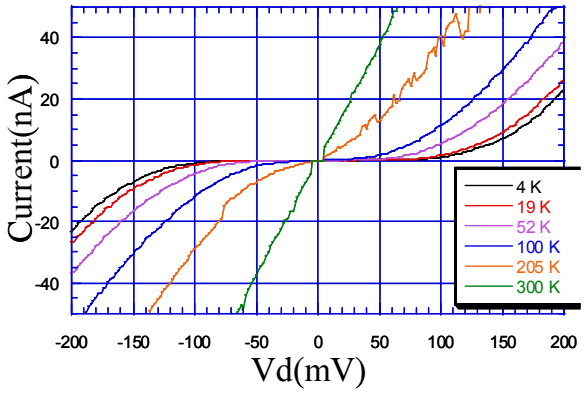

Fig.1: I_D-V_D curve of a 2µm*40nm*15nm SOI wire when varying temperature. A strong non linearity is visible at low temperature.

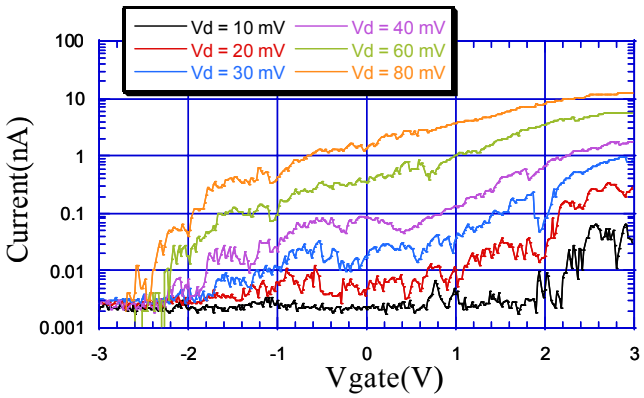

Fig 2: Gate voltage dependence of the I_{SD} current for various V_{SD} bias. Each curve is complex yet totally reproducible.

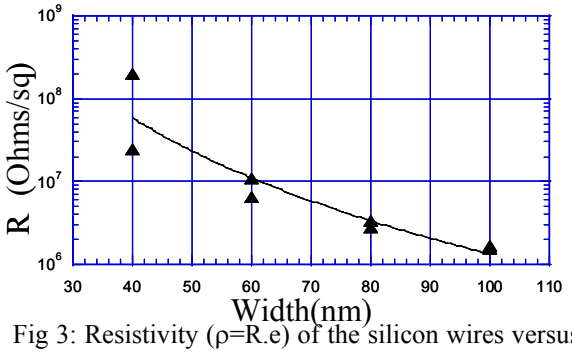

Fig 3: Resistivity (ρ=R.e) of the silicon wires versus the wire width. ρ is not constant. This could be attributed to a reduction of the effective conducting section (surface roughness) or could either be the signature of a microscopic more complex conductance law.

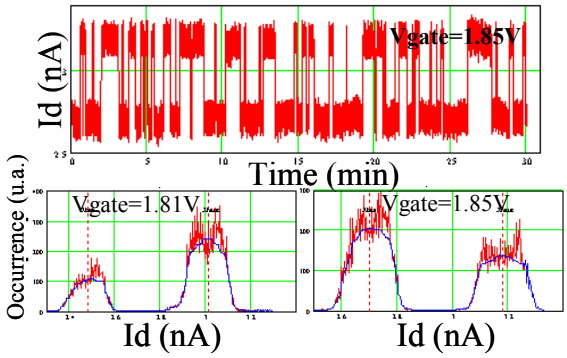

Fig.4: Time evolution of the I_{SD} current in stationary bias conditions. The evolution of the amplitude occurring for two different Gate bias is clearly visible on the histogram of the amplitude.

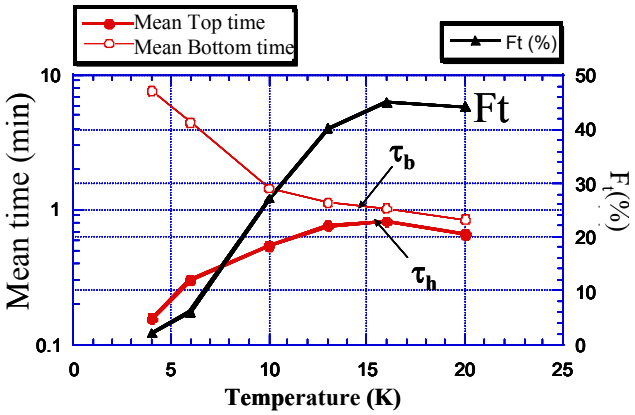

Fig.5: Temperature evolution of the top and bottom time and mean b occupation time Ft=τh/(τh+τb). This is consistent with temperature activated mechanism.

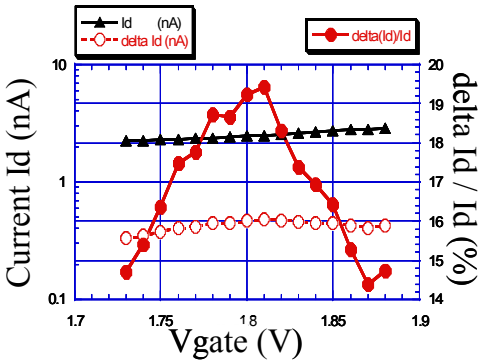

Fig.6: Gate voltage dependence of the current amplitude modulation. Note the non monotonous behaviour and the absolute level. In some cases up to 40% modulations were measured.

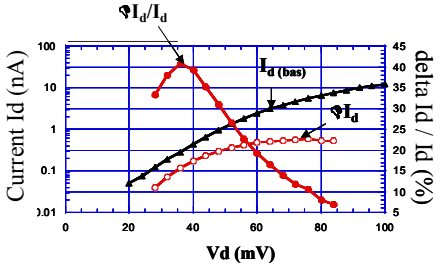

Fig.7 : Source-Drain voltage dependence of the current Id, absolute ΔId and normalised ΔId/Id current modulation.