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# Self-assembled single wall carbon nanotube field effect transistors

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***Abstract*— We report detailed characterization of *in-situ* wired single wall carbon nanotube (SWNT) field effect transistors (FETs). They were batch processed using a single step technique based on hot filament chemical vapor deposition. Raw samples show an ambipolar field effect. The temperature dependence of the gain confirms the presence of Schottky barriers at the nanotube/metal interface. Moreover the gate dependence exhibits hysteresis at any temperature due to extraction and trapping of charges. Below 30K, Coulomb blockade occurs at low drain-source bias and partially washes out the influence of the Schottky barriers.**

***Keywords- Molecular electronics, Carbon nanotubes, Self assembly, Schottky barriers.***

## I. INTRODUCTION

Carbon nanotubes are intensely studied as building blocks for nanoscale electronics. It is nowadays possible to build carbon nanotube-based integrated circuits which performances exceed those of state-of-the-art Si MOSFETs [1,2]. Applications of these devices are now being considered such as using nanotube based FETs as ultra-sensitive biological [3,4] and chemical [5,6] sensors. However the underlying physics of Carbon Nanotube Field Effect Transistors (CNFETs) is still being studied and recent results bring a new light on electron transport mechanisms in CNFETs. Martel *et al*. [7-9] have shown evidences of the existence of Schottky barriers (SB) at the metal/CN interface responsible for the field effect. CNFETs then behave as SBFETs rather than as MOSFETs, therefore the field effect depends mainly on the molecule/metal contact rather than on channel depletion. This theory is supported by the fact that many groups can interpret their data in the framework of Schottky barriers [10,11].

Most devices described in the literature are based on single nanotube manipulation or alignment techniques. These techniques are not compatible with large scale integration of carbon nanotube-based electronics. Self-assembling techniques [12,13] are promising as they allow batch-processing.

For that purpose, we have developed a self-assembling growth process based on Hot Filament assisted Chemical Vapor Deposition (HFCVD) [14], which allows low resistive in-situ wiring [15]. We present here this full process for self-assembled CNFET fabrication and the electronic measurements performed between 300 K down to 1 K.

## II. PROCESS OF SELF-ASSEMBLY

In a first stage, metallic electrodes of Ti/Co separated by a 300 nm gap have been prepatterned using conventional electron beam lithography techniques on Si wafers (highly doped silicon wafers with 0.5 µm thermal oxide). The defined location of the ultra-thin film of Co catalyst on top of the electrodes allows a localized growth of the nanotubes and the bridging and wiring of two facing electrodes by a suspended nanotube during deposition (Fig. 1). HFCVD is performed in a quartz furnace and begins with an annealing in a hydrogen atmosphere. The carbon feedstock is then provided by a gas mixture of 5-20% methane highly diluted in hydrogen. The substrate is heated up to 800°C and the filament reaches 2000-2100°C [14].

## III. STRUCTURAL CHARACTERIZATION OF SWNT FETS

Non-invasive Raman micro-spectroscopy characterization combined with TEM imaging have established the growth of highly pure SWNTs with an average diameter of 1.2 nm (Fig. 2) [16]. Moreover SEM micrographs (Fig. 1) show that the SWNTs self assemble and wire simultaneously between metallic electrodes and form suspended bridges of small bundles or even single isolated SWNTs [16]. The nanotube density and diameter can be tuned depending on the HFCVD parameters and the Co layer thickness. The high filament temperature ensures the presence of atomic hydrogen which is assumed to play a crucial role in the purity of the nanotubes. It also favors the formation of titanium carbide at the nanotube/metal interface [8] which allows a good electric contact [17].

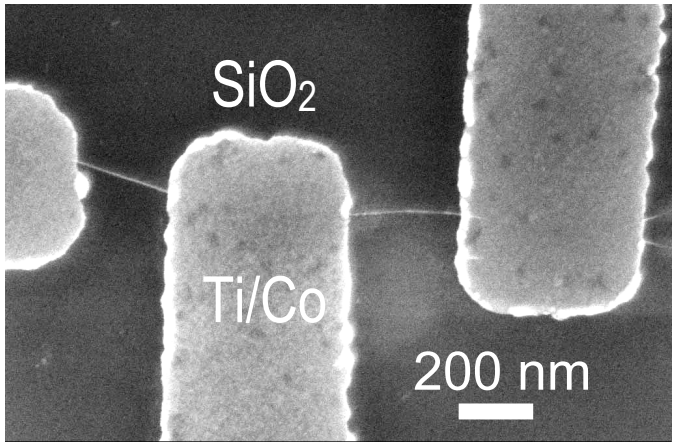


Figure 1. Scanning electron micrograph of SWNTs linking pre-patterned titanium contacts in a 4-wire geometry.

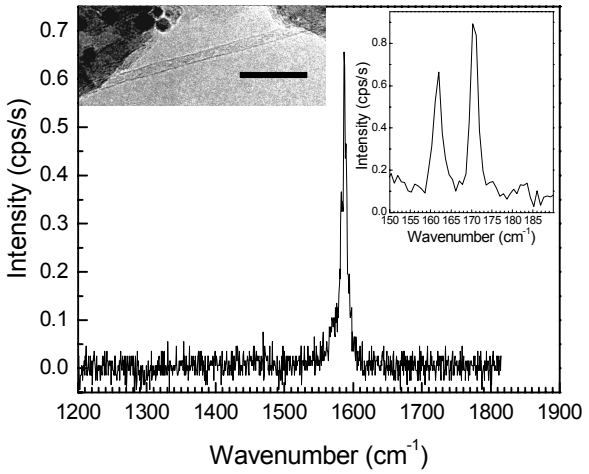


Figure 2. Raman spectrum of the core active area of a 4-wire CNFET. Upper right inset: zoom of low frequency RBM modes. Upper left inset: TEM image of a self-assembled single-walled carbon nanotube (scale bar is 5 nm).

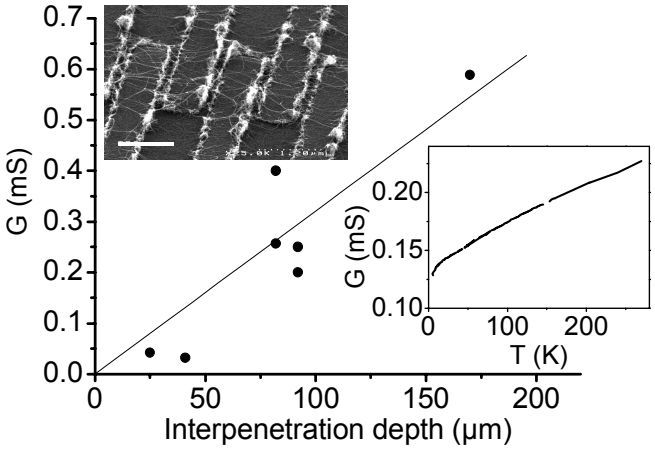


Figure 3. Dependence of 2-wire conductance at 300 K of SWNT on the brush interpenetration depth. Upper inset: scanning electron micrograph of SWNTs linking pre-patterned titanium contacts in a brush-like geometry (scale bar is 1μm); lower inset: conductance versus temperature for 50 mV bias voltage.

Fig. 2 shows a Raman spectrum taken with a 633 nm laser radiation focused on the core of a typical self-assembled CNFET. The very low signal intensity suggests there are only a few isolated or at least a single nanotube of very high cristallinity as no D-band at 1320 $cm^{-1}$ is observed [16]. The TEM image of a single SWNT grown on a TEM grid covered with Co in the same conditions in inset of Fig. 2, confirms our technique is able to grow isolated SWNTs. The presence of Radial Breathing Modes (RBM) at low frequency proves the nanotubes are single-walled and the peaks frequencies give a diameter of about 1.5 nm assuming that the RBM frequency $\omega$ is related to the diameter $d$ by the formula [18] $\omega=248/d$. Moreover the narrowness (~10 $cm^{-1}$) of the so-called G-band at 1587 $cm^{-1}$ indicates the presence of a semiconducting SWNT.

## IV. ELECTRICAL CHARACTERIZATION

We present here electron transport measurements on as-grown samples. As no post-treatment was performed, we expect our samples are free of defects or impurities that are induced by sonication or chemical purification.

Electrical characterizations were conducted between 1K and 300K using both DC measurements and low frequency lock-in detection technique. The gate was obtained by biasing the Si substrate. Two kinds of electrode configurations were used: firstly a brush-like geometry which aims to maximise the number of SWNTs bridging between contacts and secondly a 4-wire geometry which allows measurements down to a single SWNT.

At room-temperature, all tested samples show purely ohmic behavior in both tested geometries with resistances ranging from 2 kΩ to 1 MΩ.

Variation of the teeth inter-penetration length in brush geometry leads to a linear increase of the conductance with the effective surface of the electrodes facing each other (Fig. 2) which can be inferred to parallel carbon nanotube connections. At low temperatures, *I-V* curves present an increased resistance and a non-linearity in the range [-20 meV, 20 meV]. This non linearity at low $T$ can be related to the influence of energy barriers at the metal/NT interface. Considering the linear dependence of the conductance with temperature (Fig. 3 lower inset), the high number of SWNT connections (Fig. 3 upper inset), and assuming a continuous distribution of barriers Δ, the conductance can be approximated to :

$$G \propto \int_0^{+\infty} e^{-\frac{\Delta}{kT}} d\Delta \propto kT$$

With this huge number of SWNT connections in parallel, we found that applying even a large backgate voltage did not produce any change of the *I-V* characteristics. The field effect related to the semiconducting SWNTs is not seen here because it is washed out by the contribution of metallic SWNTs.

Lowering the methane proportion in hydrogen to 8 vol. %, while keeping the other synthesis parameters identical, has allowed us to decrease the number of SWNTs bridging the titanium contacts (Fig. 1).

For all 4-wire geometry samples, drain-source *I-V* curves are always found linear at room temperature up to 1 V drain-source bias with two-wire resistances ranging from 10 to 500 kΩ depending on the SWNT density and HFCVD parameters, whereas they show increasing non-linearity with decreasing temperature. Whatever the temperature, a field effect is observed on 80% of the more than 50 tested 4-wire samples (Fig. 4). Raman microspectroscopy [16] confirms the abundance of semiconducting SWNTs similarly as CNFETs obtained using other CVD methods [2, 19]. The ratio between the current in the on-state and the off-state ($I_{on}/I_{off}$) is sample dependent and varies from 1.25 to $10^4$ at room temperature (and can reach $10^6$ at 4K, see Fig. 5). Moreover our samples show ambipolar behavior at any temperature with a p-type branch more pronounced than the n-type one. Such ambipolar effect was not seen before on as-grown self assembled CNFETs but only on post-connected [20] or post-annealed devices [8,2]. Since oxygen adsorption is expected to p-dope air-exposed-CNFETs, the observed ambipolar behavior of our

CNFETs is attributed to the reductive hydrogen atmosphere during growth that could passivate the device.

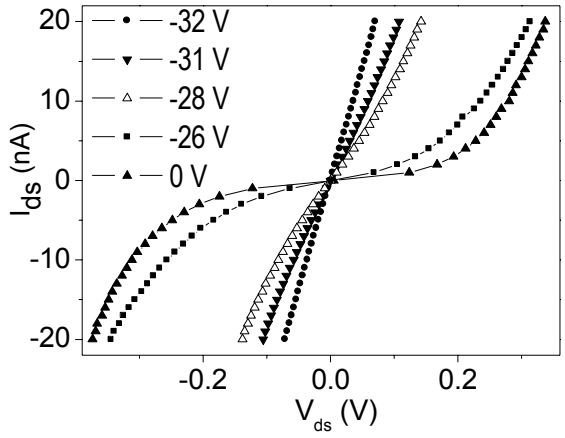


Figure 4. *I-V* curves of a CNFET in a 4-wire geometry measured at 4 K for different backgate voltages (0 to -32 V).

Additionally, we observe a strong hysteretical dependence of the drain-source current with the gate voltage sweep direction (Fig. 5). This hysteresis is caused by charge trapping in the SWNTs vicinity that partially screens the applied electric field. The loop direction indicates electrons are extracted from the SWNTs for the p-type branch (and holes for the n-type one). This effect is confirmed by discrete steps in the hysteresis at low temperature which feature small amount of charge transfer analogous to the one occuring in single electron memories [21, 22]. Moreover such a hysteresis allows to run such CNFETs as memory elements [23-25]. Applying a voltage pulse on the gate allows to switch the device between its on and off states. This is analogous to the writing-erasing of a bit in a non volatile charge-storage memory. We were able at room temperature and in ambient air to write-erase "bits" using 34 V pulses of 10 ms long (Fig. 5 inset).

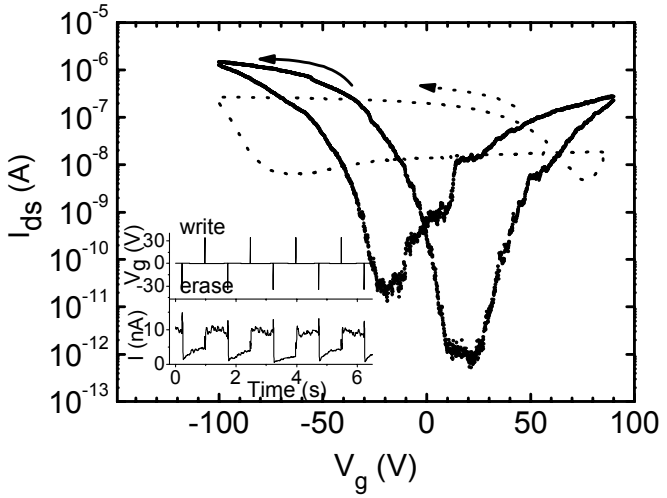


Figure 5. Gate dependence of the drain-source current at different temperatures and bias (dotted line $T$=300K $V_{ds}$=50mV, solid line $T$=1K and $V_{ds}$=+1V, sweep rate=0.05V.s-1). Arrows indicate the hysteresis direction. Inset: writing-erasing of a "bit" in a "CNFET memory" at 300 K in ambient atmosphere by applying gate voltage pulses of 34 V and 10 ms long at 300 K for a drain-source bias voltage of +40 mV. The CNFET exhibits a relaxation times of about 0.9 s before reaching a stable "on" or "off" state .

Moreover the devices showed to endure high current densities compared to standard FETs. We progressively increased the voltage applied to a CNFET up to its destruction. Fig. 6,left shows two titanium electrodes connected with suspended SWNTs bundles. Fig. 6,right shows the same area after having applied up to 60 V and 1 mA between the electrodes. The nanotubes finally broke in the middle leaving two remaining parts still wired to the electrodes and separated by a few nanometer gap. This sharp gap is an interesting structure to self-assemble and directly electrically characterize functionnalized junctions. We observed that electron transport in our CNFETs depends strongly on temperature, which is clearly seen on Fig. 3. At 50 K, the current is a quadratic function of the voltage [26], while at 4 K, all samples exhibit a zero conductance gap with a sample-dependent width varying between 30 meV and 600 meV.

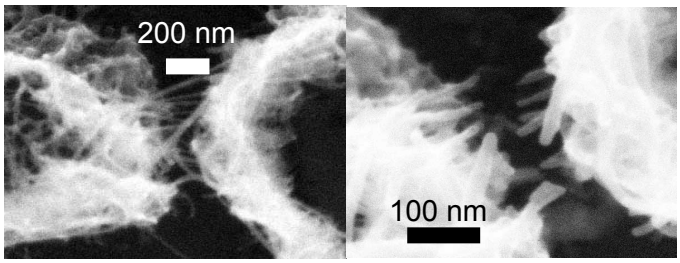


Figure 6. SEM micrographs of two titanium electrodes connected by suspended bundles of SWNTs (left) and the same area after burning the nanotubes with 60 V/1 mA (right).

Fig. 7 shows the Arrhenius plot of significant parameters that put to the fore the different transport mechanisms at different temperatures. We observe that the drain-source current follows an Arrhenius law over 30 K with 6 meV effective energy. This effect with the fact that the room temperature *I-V* curves were always found linear are consistent with tunneling through the logarithmic tail of 1D Schottky barrier [9]. It thus confirms the fact that the field effect originates from Schottky barriers at the nanotube/metal interface.

Below 30K, we observe two different behaviors that can be characterized by the gate swing $S=dV_g/dlogI_{ds}$. For large drain-source voltages $V_{ds}$, $S$ saturates at low T as it is expected for SBFETs (Fig. 7), whereas it increases abruptly for small $V_{ds}$. Moreover the drain-source current $I_{ds}$ versus gate voltage exhibits aperiodic fluctuations around the threshold voltage. Conductance peaks are correlated between traces taken at different drain source biases and exhibit a local periodicity of 300 mV [26]. Additionally, the *I-V* curves show a very large zero conductance gap of about 600 meV. Such a wide Coulomb gap and aperiodic conductance fluctuations reveal Coulomb blockade in a multiple island network as it is observed in silicon nanowires along which dopants create potential barriers [27]. Lowering the temperature reveals barriers along the SWNT channel forming a multiple tunnel junction array [28]. The junctions in series thus enlarge the effective Coulomb gap [27,29] and below 30K electron transport is dominated by Coulomb blockade at low drain-source biases. The gate effect is then reduced and $S$ increases. On the contrary, large $V_{ds}$ put the device out of the Coulomb gap where Coulomb blockade

vanishes. Schottky barriers remain then preponderant leading to saturation of S at low temperature.

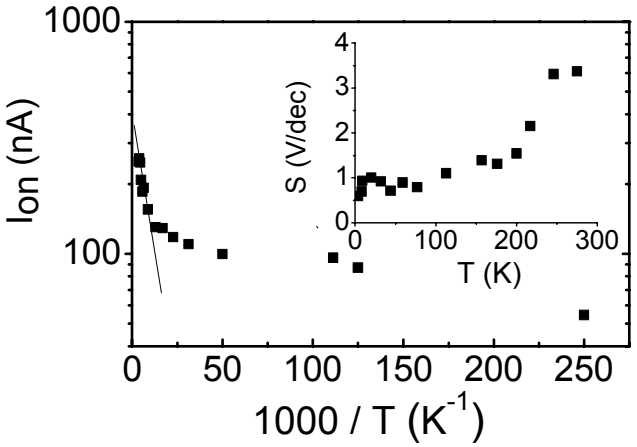


Figure 7. Arrhenius plot of the drain-source DC current in the "on" state taken at $V_g$= -15 V, $V_{ds}$=10 mV; Inset: Temperature dependence of the subthreshold swing $S=dV_g/dlogI_{ds}$. measured at drain source voltage $V_{ds}$=500 mV.

## V. CONCLUSION

We have demonstrated the simultaneous wiring and self-assembling of CNFETs using a single step procedure based on the HFCVD technique. Our CNFETs showed to be ambipolar with a strong hysteresis suitable for memory operation. Detailed low temperature characterization shows that electron transport mechanisms are in agreement with the model of Schottky barriers.

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