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# Self-Assembly of Carbon-Nanotube-Based Single-Electron Memories**

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*We demonstrate the wafer-scale integration of single-electron memories based on carbon nanotube field-effect transistors (CNFETs) using a process based entirely on self assembly. First, a "dry" self-assembly step based on chemical vapor deposition (CVD) allows the growth and connection of CNFETs. Next, a "wet" self-assembly step is used to attach a single 30-nm-diameter gold bead in the nanotube vicinity via chemical functionalization. The bead is used as the memory storage node while the CNFET operating in the subthreshold regime acts as an electrometer exhibiting exponential gain. Below 60 K, the transfer characteristics of gold–CNFETs show highly reproducible hysteretic steps. Evaluation of the capacitance confirms that these current steps originate from the controlled storage of single electrons with a retention time that exceeds 550 s at 4 K.*

**Keywords:**
- chemical vapor deposition
- coulomb blockade
- field-effect transistors
- nanotubes
- self-assembly

## 1. Introduction

Single-electron devices could be a possible breakthrough for tomorrow's nanoelectronics.[1] Indeed, the fundamental quantization of electric charge could be used to code and process digital information. Reduced power consumption, and large-scale integration are among the many advantages. The most promising single-electron device for a broad range of applications is the single-electron memory.[2] The single-electron memory can be seen as the ultimate miniaturization of the flash memory for which Coulomb blockade can lead to multilevel coding functionality.[3] In this device, Coulomb blockade introduces additional rules that allow an external gate to control the exact number of excess electrons in the storage node. This node consists of a small capacitance electrode (the so-called "island"), which acts as a charge trap. When placed in the Coulomb blockade regime the island can exchange electrons one by one via tunneling with a charge reservoir. To allow the charge readout, the island is capacitively coupled to a charge-sensitive amplifier device (the so-called "electrometer") that must have sub-electron charge sensitivity.[4] The electrometer can be implemented either by a single-electron transistor (SET), as in the original experiments,[2] or by a highly sensitive field-effect transistor (FET).[3] Many kinds of electrometers have been implemented so far, that involve metallic electrodes,[2] semiconducting electrodes,[5] and more recently single-walled[6,7] or multi-walled[8] carbon nanotubes as the active channel.

To date, fabricating a single-electron memory has involved at least one electron beam lithography and mask

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alignment step, thus not allowing for low-cost, large-scale integration. In this paper, we present a method based on self-assembly that allows the successful parallel integration of single-electron memories for which the island is implemented by a gold nanocrystal and the electrometer by a carbon nanotube FET (CNFET).

## 2. Results

### 2.1. CNFET Integration and Functionalization

The CVD growth of carbon nanotubes using catalyst-covered electrodes has proven to be a powerful method to achieve the full integration of CNFET devices.[9] In our process, we perform this template-directed growth using a hot-filament-assisted CVD method.[10] The growth parameters are adjusted to reach the limit of an individual carbon nanotube or bundle connection per electrode pair.[11] This technique allows simultaneous self-assembly and electrical connection during the nanotube synthesis. Both unipolar and ambipolar CNFETs[12] are obtained with a yield that exceeds 50% on the 9000 electrode pairs. As confirmed by TEM and AFM measurements (see Supporting Information), our synthesis method leads to SWNTs that have relatively large diameters (often exceeding 1.5 nm) with a probable high occurrence of double-walled carbon nanotubes. Semiconducting nanotubes will then have a bandgap in the range of 0.4–0.6 eV,[13] which is almost half of what is currently seen in CVD-prepared SWNTs. Because of their relatively small bandgap, these nanotubes, as is the case for double-walled carbon nanotubes,[14] are quite sensitive to electrostatic doping, for both positive and negative gate voltages yielding to a large occurrence of ambipolar CNFETs.[15] In our batches, more than half of the connected circuits exhibit an ambipolar field effect, which is significantly higher than those prepared by the other CVD methods.

For the deposition of the colloidal gold beads, a standard silanization of the silica substrate is employed. This silanization process induces a net positive charge on the substrate by grafting amine groups on to the silicon oxide of the wafer surface. Such surface functionalization is known[16] to lead to a well-pronounced charge transfer that enhances the p-type behavior in the already p-doped CNFETs, as shown in Figure 1.

Compared to the field effect measured before silanization, threshold voltages are shifted towards negative gate voltages. Moreover the saturated "On current" on the p side (negative gate voltages) increases by 100% at 4.2 K, while the current on the n side decreases by the same amount. Once the CNFETs fabricated by the "dry" self-assembly step are fully characterized, we proceed to the second self-assembly step, which involves a "wet" coupling of a single gold nanoparticle to each CNFET. A relatively large diameter (30 nm) was chosen for reproducibility and for increased electrostatic coupling. By varying the colloid concentration we can obtain a bead density of about 1 $\mu m^{-2}$, which leads on average to a single bead coupling per

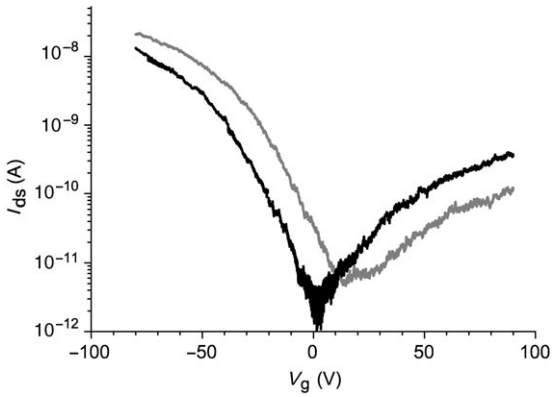


**Figure 1.** Current versus gate voltage of a typical, 1-μm-long self-assembled CNFET before (black curve) and after (gray curve) silanization of the silica substrate measured at low temperature (4 K). The drain–source voltage is 2 V while the gate voltage was applied using silicon back-gating. The positive charging of the substrate induced by the surface functionalization induces a charge transfer seen as an effective p-type doping of the CNFET. The same effect is seen at room temperature but is less pronounced.

CNFET (See Figure 2). Even with such a low surface coverage, the nanotube–colloid distance was found to be around 10 nm in most cases. Grafting of aminosilane in our process

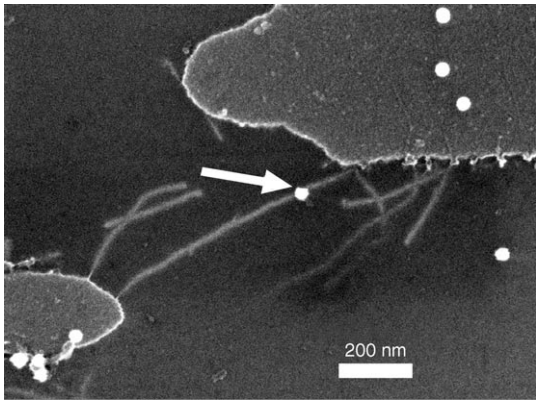


**Figure 2.** Scanning electron micrograph showing a typical self-assembled carbon-nanotube-based single-electron memory. It is shown after the two self-assembly steps but before parylene encapsulation and top-gate deposition. The nanotubes are lying on the silanized silica substrate and a single 30-nm-diameter gold nanocrystal (arrow) has been deposited.

leads to a relatively thick capping layer on the silica and on the nanotube. The good adhesion probability of the bead near the nanotube is attributed to the combined effects of the surface roughness created near the nanotube and to the presence of amine groups on the nanotube.

### 2.2. Electrical Characterization of the Memory Effect

For characterization, the memory device (see Figure 3) is encapsulated within a 100-nm-thick parylene C dielectric layer, a material well suited for deposition on top of molec-

  

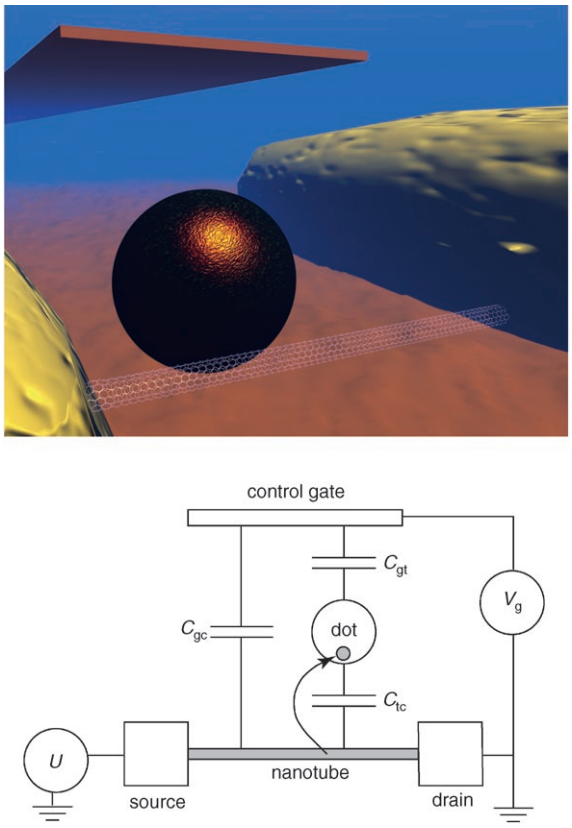


**Figure 3.** Top: Artist's impression of the nanotube-based memory device. The nanotube electrometer is self-assembled via the HFCVD technique between metallic electrodes (note that the relative heights of the nanotube electrodes and the gold bead are to scale). The colloidal gold nanocrystal is self-assembled by a physicochemical process. A top gate is realized above the gap between the electrodes. Bottom: Equivalent electrical circuit showing the different capacitances involved in the gate coupling of the nanotube in the memory device. Charge transfer occurs between the nanotube and the gold nanocrystal, as shown by the arrow.

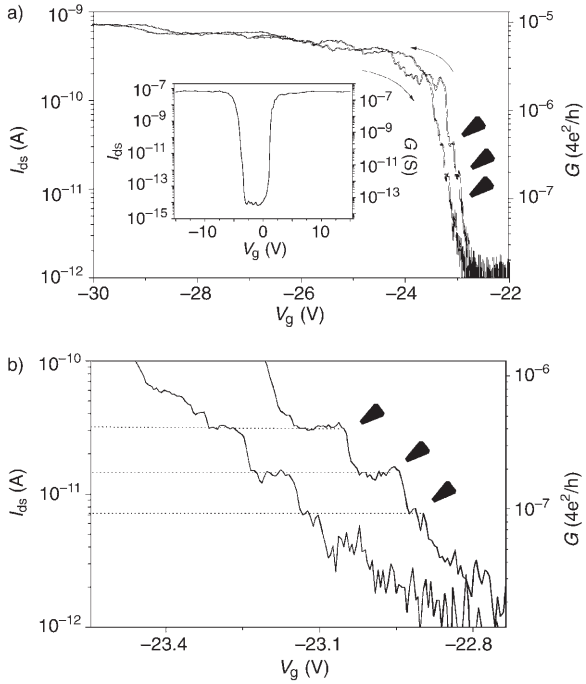


**Figure 4.** a) CNFET current versus gate voltage at 2.2 K for a typical device (sample A). The curve is plotted at $V_{ds} = 500$ mV for opposite gate sweeps of $\pm 0.5$ Vs$^{-1}$. Inset: Transfer characteristic of a control CNFET sample from the same batch but without gold functionalization for which no current step is observed. The drain–source current was measured at $T = 6$ K and for a drain–source voltage $V_{ds} = 500$ mV. The gate voltage was applied on both the top and the back gates with a sweep rate of $-0.1$ Vs$^{-1}$. The characteristic exhibits symmetric p- and n-type branches showing an ambipolar behavior. b) An expansion on the above curve in the subthreshold regime. On this semi-logarithmic scale, the nanotube current exhibits regularly spaced steps in both *x* and *y* directions, a signature of a constant amount of charge transfer between the nanotube and the gold bead.

ular devices.[17] Finally a gate electrode was deposited on top to increase the gate coupling. No nanotube–gate leakage was measured using the top gate, due to the parylene layer, which allows a highly conformal deposition of the dielectric film.

Below 120 K, the field effect exhibits steps that become hysteretic below 60 K. These steps are direct measurements of the charge transfer that occurs between the CNFET and the gold bead. This is confirmed by the fact that no steps are observed for transistors without the gold bead attachment (Figure 4a, inset).

For a 30-nm-diameter gold bead, the self capacitance $C_{self} = 4\pi\varepsilon_0\varepsilon_r r = 5.3$ aF (with sphere radius $r = 15$ nm and the parylene C dielectric permittivity $\varepsilon_r = 3.2$). The charging energy is $E_c = e^2/2C_{self} = 15$ meV, equivalent to a temperature of 180 K. At temperatures well below this limit, Coulomb blockade dominates electron transport, so that single electrons transit between the channel (i.e., the CNT) and the floating dot (i.e., the gold bead) through a thick junction (either multiple tunnel junctions or a Fowler–Nordheim field-emission barrier).[18] The transfer then occurs at regularly spaced gate voltages separated by $\Delta V_w$ (Figure 5) where $e\Delta V_w$ corresponds to the work from the voltage source necessary to add or remove charge quanta from the

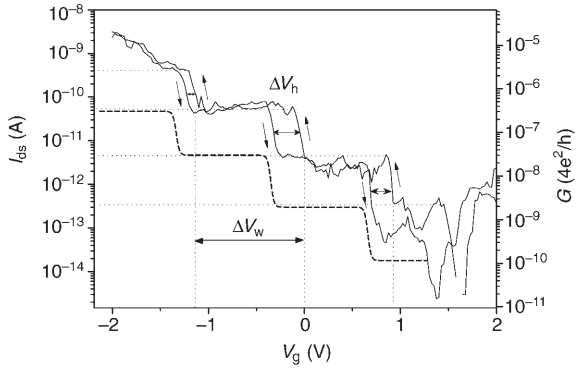


**Figure 5.** Memory operation of a second gold-functionalized CNFET device (sample B) probed in the subthreshold regime at $T = 2$ K with a low sweep rate of 10 mVs$^{-1}$. Dotted line: a fit (shifted for clarity) obtained from Equation (2) for the Coulomb staircase of an electron box. The charging energy of the fit is 80 K. Time retention of an electron in the gold beads exceeds 550 s.

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bead. The charge stored in the bead induces a local electrostatic field on the nanotube, which in turn modifies its conductivity. The CNFET thus acts as an electrometer probing the charge present on the bead. This phenomenon is reminiscent to what occurs in CNFET-based electrochemical transducers,[19] for which metal particles can be coupled to the CNFET channel to make the sensing properties chemically specific.[20]

In the subthreshold region, the CNFET transconductance response is exponential:

$$\Delta I_{ds} = \frac{1}{S(T)} \exp\left(\frac{C_{gc}\Delta V_g}{e}\right), \quad (1)$$

where $S(T)$ is the temperature-dependent subthreshold slope. Therefore any electrostatic charge modification in the bead will be exponentially amplified. Indeed, this amplification originates from the fact that the current through the nanotube is established via quantum electron hopping,[12,21] which can be affected by the local electrostatic environment.[22,23] This exponential behavior in the substhreshold regime allows the observation of regularly spaced current steps in plots of $\log(I_{ds})$ versus $V_g$ (see Figures 4 and 5), contrary to its operation in the saturation region (between $-30$ V and $-24$ V on Figure 4) for which the charge sensitivity rapidly drops.

A precise analysis of the memory operation is provided for sample B (Figure 5). In this device, the CNFET current steps occur at regularly spaced gate voltages $\Delta V_w = 0.93 \pm 0.07$ V, and each current step is about 1 decade in height. This is sensitive enough for detecting even the inherently low channel currents circulating in the subthreshold regime. As expected, this charge trapping is not symmetrically reversible: the charging/discharging of the trap occurs at a gate voltage separated by $\Delta V_h$. The induced hysteresis depends on the temperature and on the gate voltage sweep rate. Indeed, charge retention in the Coulomb blockade regime is easily affected by thermal activation.[23] At low temperatures ($T \approx 2$ K), the hysteresis in $\Delta V_h$ is relatively constant even for a low sweep rate (Figure 5). Its value $\Delta V_h = 0.18 \pm 0.10$ V has been measured between two corresponding steps on the gate sweeps. These steps correspond to the trapping an detrapping of the same excess charge on the particle and are separated by a time $\tau$ related to the sweep rate and cycle amplitude. We have measured the current at a very slow sweep rate of $\pm 10\ \mathrm{mV\,s^{-1}}$, and for a hysteresis cycle down to $V_g = -2$ V, which implies $\tau$ is longer than 550 s. This time corresponds to the retention time of the charge before it is transferred away from the particle. This shows that the operation time of our memory can be longer than 550 s.

In order to provide further evidence to support the fact that the gold bead is involved in the charge transfer, we have measured the temperature dependence of the memory effect in sample A. For that experiment we have swept the gate at a large amplitude, thus leading to a threshold voltage that is significantly shifted from those shown in Figure 4 on the same sample. Sharp steps due to discrete charge transfers vanish gradually as the temperature approaches the 100–150 K region. The inset shows a detail of a step showing the disappearance of the hysteresis that occurs at a lower temperature (60 K) than the total thermal smearing of the charge step (above 90 K).

## 3. Operation of the Memory at the Single-Electron Limit

In the low-temperature regime $k_B T/E_c \ll 1$, the charge step depicting a single electron charging event ($m \rightleftharpoons m+1$) for a single electron box can be written as:[24]

$$\langle n \rangle = m + \frac{1}{2}\left\{1 + \tanh\left[-\frac{E_c}{k_B T}\left(m + 1/2 - \frac{C_{gt}V_g}{e}\right)\right]\right\}, \quad (2)$$

where $\langle n \rangle$ is the average number of excess electrons in the dot at a finite temperature $T$, and $m$ is the integer number of excess electrons in the dot ($m \le \langle n \rangle \le m+1$). This result is valid up to $E_c/k_B T \approx 0.2$.[25]

From that equation, we deduce that the maximum slope of the Coulomb staircase is given at the point for which the argument of the hyperbolic tangent cancels to zero:

$$\left[\frac{\partial\langle n \rangle}{\partial(C_{gt}V_g/e)}\right]_{max} = \frac{E_c}{2k_B T} \quad (3)$$

One can see from this result that a noticeable thermal smearing of the Coulomb staircases occurs rapidly when the ratio $k_B T/E_c$ exceeds 0.1.[24] A fit of the Coulomb staircase at the lowest temperature (2 K) taking into account the exponential gain of the nanotube electrometer is shown in Figure 5. The fitted charging energy (80 K) underestimates the predicted charging energy of the bead (180 K). Several reasons can lead to such a discrepancy, but the major uncertainty is likely to come from spurious heating effects, which are likely to occur in a cryogenic probe at such low temperatures.

To further investigate the thermal smearing of the discrete charge steps, we have measured the temperature dependence of the transfer characteristic of the nanotube $I_{ds}(V_g)$ for sample A (Figure 6). As expected, the sharp steps due to discrete charge transfers vanish gradually as the temperature reaches the 100–150 K region. Charge transfer involving surface contaminants would have persisted up to much higher temperatures.[26]

A closer analysis of the hysteresis can give a quantitative estimate of the transferred charge. The step parameters $\Delta V_w$ and $\Delta V_h$ characterize the charge increase and directly depend on the different coupling capacitances in the circuit and on the number $n$ of electrons transferred to or from the gold bead. This allows us to confirm the device is operating at the single-electron limit by evaluating $n$ from the equation system:[26]

$$\begin{cases} \Delta V_w = \frac{ne}{C_{gt}} \\ \Delta V_h = \frac{neC_{tc}}{(C_{tc}+C_{gc})C_{tot}} \end{cases} \quad (4)$$

  

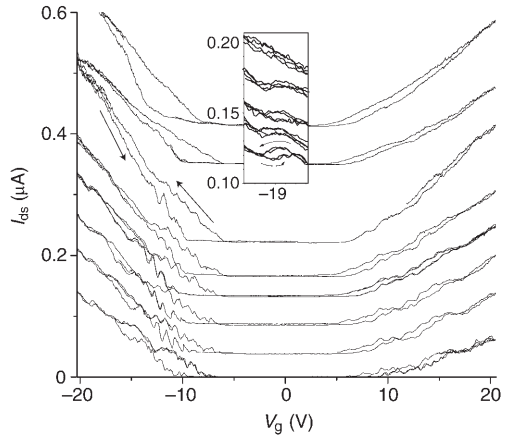


**Figure 6.** Temperature dependence of the transfer characteristics ($I_{ds}$–$V_g$) for the memory (sample A). Curves are measured at $V_{ds}=300$ mV for high-speed gate sweeps of 5 $Vs^{-1}$. The curves are shifted for the sake of clarity. From bottom to top, the temperatures are 15, 52, 60, 70, 90, 130, 160, and 225 K. Current measurements at 160 and 225 K have been vertically rescaled by a factor of 1/2. Inset: Expanded data around $V_g=-19$ V for the four lowest temperatures.

where $C_{tot}$ is the total gate-device capacitance given by:

$$C_{tot} = C_{gc} + \frac{C_{tc}C_{gt}}{C_{tc}+C_{gt}} \quad (5)$$

Considering the presence of Schottky barriers at the nanotube–electrode contacts,[27] one should expect the gold bead to exert an influence on the nanotube conductivity only if located near the metal–nanotube interface. However, we observe the charge steps independent of the bead position along the nanotube. Additionally, the current does not vary between two discrete steps and does not exhibit the characteristic slope of the field effect. At higher temperatures (around 10 K), the bead screening becomes less efficient and the staircases start to bend and rapidly become equal to the average subthreshold slope. This suggests that the sensing part of the CNFET is very temperature dependent, and that at low temperatures the sensing area can be efficiently screened by the gold bead. The disorder along the nanotube length induces quantum dots connected in series,[12] through which the electrons transit according to Coulomb blockade rules. Therefore, the charge on the gold bead controls the electron percolation through the CNFET via electrostatic action on a single quantum dot barrier. This specific dot acts as a filter for the whole device. It is then reasonable to assume that $C_{tc} >> C_{gt}, C_{gc}$, which allows us to simplify the equations accordingly: $C_{tot} = C_{gc} + C_{gt}$, and $\Delta V_h = \frac{ne}{C_{gc}+C_{gt}}$.

These equations give the formula for $n$:

$$n = \frac{\Delta V_h C_{gc}}{e\left(1-\frac{\Delta V_h}{\Delta V_w}\right)} \quad (6)$$

$C_{gc}$ is the capacitance between the nanotube intramolecular quantum dot and the gate. This parameter depends on the quantum dot size, which here is difficult to estimate without precise control experiments such as scanning gate microscopy[26] or Coulomb blockade measurements. Devices from other batches have been measured at very low temperatures (70 mK), which has allowed a determination of the intramolecular quantum dot sizes from their charging energy and excited states (see Supporting Information). We thus assume the dot size $L$ in this memory device is equal to the mean size obtained from other devices: $L \approx 64 \pm 50$ nm (such an assumption introduces a large uncertainty). $C_{gc}$ is then calculated using the geometric configuration of the gate:

$$C_{gc} = L\frac{4\pi\varepsilon_0\varepsilon_r}{2\ln\left(\frac{h+\sqrt{h^2-a^2}}{a}\right)} \quad (7)$$

where $h$ is the dielectric thickness and $a$ is the nanotube radius. For sample B, the post-measurement scanning electron microscopy observation of the device revealed a misalignment of the top gate inducing a very weak top-gating. Therefore, we only consider the back gate in the following calculations: $h$ is then equal to 1 μm $SiO_2$ for which $\varepsilon_r=3.9$. We then obtain $C_{gc}=1.9\pm1.5$ aF, and from Equation (5) we deduce an approximate number of transferred electrons of $1 \le n \le 8$. The large uncertainty comes from the cumulative uncertainty of each experimentally measured quantity, especially the charge retention hysteresis $\Delta V_h$. This interpretation within the framework of Coulomb blockade theory confirms the fact that this device involves a few electrons in each charge transfer, in contrast to the thousands of electrons trapped in a conventional flash memory. Considering that each step has a constant height and width in the semilogarithmic plot (Figure 5), the amount of charge transferred is constant, which most probably is equal to a single charge quantum.

## 4. Conclusion

In conclusion, this experiment provides a successful integration (on a wafer scale) of self-assembled single-electron memories working at liquid helium temperatures. The double self-assembly process allows the controlled integration of both carbon nanotubes and floating gold dots on the device. Analyses of the temperature behavior of the charge-step hysteresis have shown that single-electron transfer events to and from the gold bead are clearly observed.

A better control of the gold bead position would reduce the dispersion of the island–electrometer coupling values. Moreover, reducing the size and thus the charging energy of the particle would increase the operation temperature, which could reach 300 K. At low temperatures, the particle is coupled with the nearest quantum dot in the nanotube. Even though the single-electron effect can subsist at 300 K in nanotubes exhibiting dense defects,[28] electron transport in CNFETs is mostly controlled at room temperature by the Schottky barriers at the contacts. Placing the nanoparticle close to it, for example by controlled hydrophobic interac-

  

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tions[29] that allow specific attachment on the nanotube channel could be used to realize a similar device.

## 5. Experimental Section

*Substrate preparation*: We started from a 2-inch-diameter degenerately doped silicon wafer. The wafer was thermally oxidized to obtain a 1-μm-thick silica top layer, which acts as the backgate dielectric. Sub-micrometer metallic electrodes were prefabricated using standard deep-UV lithography followed by electron beam evaporation and lift-off. The electrodes were made of a 30-nm-thick titanium layer covered by a thin film of cobalt (3 nm thick) that served as a catalyst template for the nanotube chemical vapor deposition (CVD). The electrodes were separated by a 0.6–1.2 μm gap.

*CNFET fabrication*: CVD deposition was carried out using $CH_4$ (5–20 vol.%) in hydrogen at a total pressure of 30–100 mbar. The substrate was maintained at 750–850 °C. The tungsten filament, placed 1 cm above the substrate, was heated to 1900–2100 °C. During the synthesis, in situ reflectivity measurements and the intensity of elastically scattered and reflected light from a 633 nm laser gave insight into real-time growth kinetics.

*CNFET functionalization*: For the silanization of the substrate, the wafer was dipped in (3-aminopropyl)triethoxysilane (Sigma-Aldrich) diluted to 1% in deionized water for 1 h. This procedure yielded an amine coating over the whole sample of a few nanometers thickness, which is thick enough to embed the nanotubes. For gold nanoparticle attachment on the CNFET, an aqueous solution of colloidal gold (Ted Pella, Inc., Redding, CA) was used, which was diluted in 10 equivalents of water. A film of colloidal gold solution was deposited on half of the CNFET wafer and incubated for 5 min. The wafer is then gently rinsed in ultrapure water. The other half of the wafer was left free from colloidal gold in order to provide control samples.

Encapsulation was performed with a film of parylene C deposited by cold CVD in a Labtop Model 3000 from Para-Tech. Finally, top-gate electrodes aligned above the nanotubes were fabricated by UV lithography followed by a thermal evaporation of gold (30 nm) and then by lift-off.

*Electrical characterization*: The whole wafer was placed in a cryogenic probe station (TT-prober, Desert Cryogenics, Tucson, AZ) that allows the testing of several devices while the temperature can be continuously controlled between 2 and 300 K. Very-low-temperature measurements were carried out in a He3/He4 dilution cryostat (Concept-Soudure, Echirolles, France), with shielded lines.


[1] Y. Ono, A. Fujiwara, K. Nishiguchi, H. Inokawa, Y. Takahashi, *J. Appl. Phys.* **2005**, *97*, 031101.
[2] a) T. A. Fulton, P. L. Gammel, L. N. Dunkleberger, *Phys. Rev. Lett.* **1991**, *67*, 3148; b) P. Lafarge, P. Joyez, H. Pothier, A. Cleland, T. Holst, D. Esteve, C. Urbina, M. H. Devoret, *C. R. Acad. Sci.* **1992**, *314*, 883.
[3] L. Guo, E. Leobandung, S. Y. Chou, *Science* **1997**, *275*, 649.
[4] M. H. Devoret, R. Schoelkopf *Nature* **2000**, *406*, 1039.
[5] K. Nakazato, R. J. Blaikie, H. Ahmed, *J. Appl. Phys.* **1994**, *75*, 5123.
[6] M. S. Fuhrer, B. Kim, M. T. Dürkop, T. Britlinger, *Nano Lett.* **2002**, *2*, 755.
[7] K. Tsukagoshi, E. Watanabe, I. Yagi, N. Yoneya, Y. Aoyagi, *New J. Phys.* **2004**, *6*, 3.
[8] L. Roschier, R. Tarkiainen, M. Ahlskog, M. Paalanen, P. Hakonen, *Appl. Phys. Lett.* **2001**, *78*, 3295
[9] Y.-C. Tseng, P. Xuan, A. Javey, R. Malloy, Q. Wang, J. Bokor, H. Dai, *Nano Lett.* **2004**, *4*, 123
[10] L. Marty, V. Bouchiat, A. M. Bonnot, M. Chaumont, T. Fournier, S. Decossas, S. Roche, *Microelectron. Eng.* **2002**, *61–62*, 485.
[11] L. Marty, C. Naud, M. Chaumont, A. M. Bonnot, T. Fournier, V. Bouchiat, *Nanotechnology* **2003**, *2*, 240. *IEEE-NANO 2003 Third IEEE Conference on Nanotechnology.*
[12] L. Marty, V. Bouchiat, C. Naud, M. Chaumont, T. Fournier, A.-M. Bonnot, *Nano Lett.* **2003**, *3*, 1115.
[13] H. Kataura, Y. Kumazawa, Y. Maniwa, I. Umezu, S. Suzuki, Y. Ohtsuka, Y. Achiba, *Synth. Met.* **1999**, *103*, 2555.
[14] T. Shimada, T. Sugai, Y. Ohno, S. Kishimoto, T. Mizutani, H. Yoshida, T. Okazaki, H. Shinohara, *Appl. Phys. Lett.* **2004**, *84*, 2412.
[15] L. Marty, PhD Thesis, Université Joseph Fourier (F), **2004**.
[16] S. Auvray, V. Derycke, M. Goffman, A. Filoramo, O. Jost, J.-P. Bourgoin, *Nano Lett.* **2005**, *5*, 451.
[17] V. V. Podzorov, M. Pudalov, P. N. Lebedev, M. E. Gershenson, *Appl. Phys. Lett.* **2003**, *82*, 1739.
[18] T. Futatsugi, A. Nakajima, H. Nakao, *FUJITSU Sci. Tech. J.* **1998**, *34*, 142.
[19] For a review, see : K. Balasubramanian, M. Burghard, *Small* **2005**, *1*, 180.
[20] J. Kong, K. Chapline, H. Dai, *Adv. Mater.* **2001**, *13*, 1384.
[21] P. L. McEuen, M. Bockrath, D. H. Cobden, Y.-G. Yoon, S. G. Louie, *Phys. Rev. Lett.* **1999**, *83*, 509.
[22] M. T. Woodside, P. L. McEuen, *Science* **2002**, *296*, 1098.
[23] P. D. Dresselhaus, L. Ji, S. Han, J. E. Lukens, K. K. Likharev, *Phys. Rev. Lett.* **1994**, *72*, 3226.
[24] P. Lafarge, PhD Thesis, Université Paris 6 (F), **1993**.
[25] P. Lafarge, H. Pothier, E. R. Williams, D. Esteve, C. Urbina, M. H. Devoret, *Z. Phys. B* **1991**, *85*, 327.
[26] B. M. Kim, Y.-F. Chen, M. S. Fuhrer in *Fullerenes Vol. 12: The Exciting World of Nanocages and Nanotubes* (Eds.: P. Kamat, D. Guldi, K. Kadish), ECS Conference Proceedings, **2002**, pp. 541–548.
[27] P. G. Collins, M. Hersam, M. Arnold, R. Martel, P. Avouris, *Phys. Rev. Lett.* **2001**, *86*, 3128.
[28] a) H. W. C. Postma, T. Teepen, Z. Yao, M. Grifoni, C. Dekker, *Science* **2001**, *293*, 76; b) K. Matsumoto, S. Kinoshita, Y. Gotoh, K. Kurachi, T. Kamimura, M. Maeda, K. Sakamoto, M. Kuwahara, N. Atoda, Y. Awano, *Jpn. J. Appl. Phys. Part 1* **2003**, *42*, 2415.
[29] A. V. Ellis, K. Vijayamohanan, R. Goswami, N. Chakrapani, L. S. Ramanathan, P. M. Ajayan, G. Ramanath, *Nano. Lett.* **2003**, *3*, 279.


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