J. Phys IV France **12** (2002)

DOI: 10 1051/jp420020044

Electron transport in silicon nanostructures based on ultra-thin SOI

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Abstract: We present an experimental study of ultra-thin SOI-based nanostructures The systems have a van der Pauw geometry, with a radius of 2 µm. The resistance per square $R_\square$ is first analyzed in the temperature range 300 K - 4 2 K, and for different conditions of back gate voltages ($0\ V < V_g < 4\ V$) The magnetoresistance was measured at very low temperatures ($10\ mK < T < 900\ mK$), for magnetic fields $-2500\ G < B < 2500\ G$ The experimental results exhibit a negative magnetoresistance that we attribute to quantum interference effects due to time reversed electron paths and known as weak localization Fundamental properties of the material at low temperatures such as the electron phase coherence length l_ϕ, the elastic mean free path l, and the mobility μ are then estimated throughout the obtained results

1. INTRODUCTION

Over the last 30 years, silicon-on-insulator (SOI) based devices have been widely studied, since they offer the possibility of reduced capacitance effects, and thus allow a faster operation More recently ultra-thin SOI layers have attracted much attention for implementing silicon quantum devices. A recent example is the observation of Coulomb blockade, and the realization of a Single-Electron-Transistor (SET) operating at 4 K [1,2]. However, in comparison to silicon bulk and GaAs based nanostructures, the fundamental properties of nanoscale silicon structures are not completely understood, especially at low temperatures

In this work, we report low temperature measurements of electron transport in SOI-based nanostructures, and under magnetic field ($-2500\ G < B < 2500\ G$) Specific attention has been given to mesoscopic effects observed at very low temperatures in order to evaluate the characteristic lengths of the material.

2. FABRICATION METHOD

We used n-doped silicon-on-insulator films, (100) surface oriented, and prepared with Unibond Smartcut® technology. Unlike SIMOX prepared SOI, this technology ensure both single crystal quality (no defect due oxygen implantation) [3] and a sharp silicon/buried oxide interface, as presented in Fig 1

The silicon layer was originally 200 nm thick, and the regions of interest were thinned down to 15 - 20 nm with a LOCOS process, for a buried oxide thickness of 100 nm The connexion pads were doped with a dose of $2\times10^{15}\ cm^{-2}$ by implantation of 30 keV phosphorous. The SOI layer were implanted with arsenic ions at 8 keV for a dose of $2\times10^{14}\ cm^{-2}$.

The active parts of the nanostructures were realized using e-beam lithography and/or AFM lithography The different steps of the process are presented in Fig. 2. The lateral resolution varies between 15 nm and 80 nm

3. ELECTRON TRANSPORT PROPERTIES

3.1 Resistivity measurements

The measurements have been performed on van der Pauw structures with a radius of 2 μm (see inset Fig 4). We first measured the resistance of the structures at room temperature The van der Pauw geometry is well suited for the measurement of the resistance per square R of a conductor. R is related to two characteristic resistances R_A and R_B throughout the equation [4]

$$e^{-\pi R_A/R_W} + e^{-\pi R_A/R_W} = 1 \qquad (1)$$

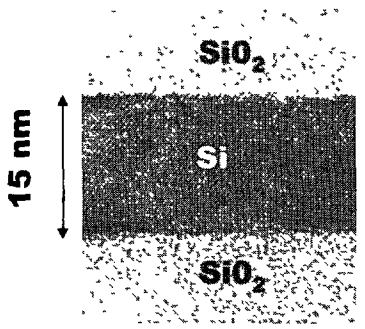

Figure 1 Schematics of the process steps used for the realization of the SOI nanostructures.

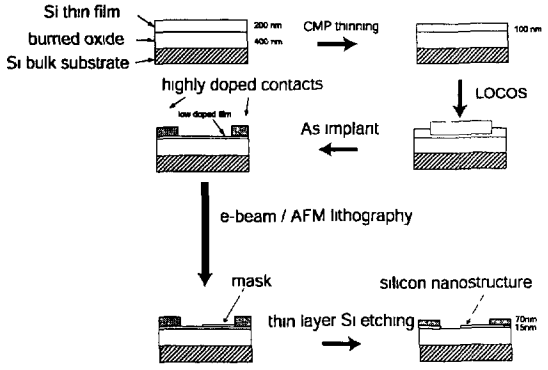

Figure 2: TEM photograph of a SiO_2 / Si interface obtained with Unibond Smartcut® technology

This equation can be solved numerically $R_A = (R_{21,34} + R_{12\,43} + R_{43\,21} + R_{34\,21})$ and $R_B = (R_{32\,41} + R_{23\,14} + R_{14\,23} + R_{41,32})$ take into account a possible asymmetry between contacts, where the resistances $R_{ij\,kl}$ are obtained for a current injected between contacts i and j, and a voltage difference measured between k and l. The numbering of the contacts is shown in the inset of Fig. 4.

At room temperature a sheet resistance of $R_\square \approx 1670 \pm 100\ \Omega$ is found, leading to a 3D resistivity of $\rho = R_\square \times e = 2.5\times10^{-3}\ \Omega$.cm, where e = 15 nm is the thickness of the silicon layer We observed that the measured resistances were independent of the configuration within a precision of 5 %, revealing a good symmetry between the contacts. Subsequently, all the measurements were performed in the same configuration, assuming that all configurations are equivalent, with $R_\square = R_{12\,43} \times \pi / \ln(2)$ [4]

3.2 Temperature dependence between 300 K and 4.2 K

The resistance per square as a function of the temperature was then measured between 300 K and 4 2 K A back gate voltage V_g between 0 and 4 V was applied on the substrate The obtained results are presented in Fig 3. At $V_g = 0$ V, the resistivity continuously decreases between 300 K and 100 K At room temperature $R_\square \approx 2.9\ k\Omega$ at $V_g = 0$ V is much higher than in the previous case where the gate was floating To apply a back gate voltage dramatically modifies $R_\square$, which decreases at 300 K Between 300 K and 100 K, $R_\square$ shows first an insulating behavior (*i.e.* the resistance increases when the temperature decreases) followed by a metallic behavior when $V_g > 0$ V. The maximum of the sheet resistance is $R_\square \approx 2.0\ k\Omega$ at $T \approx 175$ K for $V_g = 2$V, and $R_\square \approx 1.7\ k\Omega$ at $T \approx 120$ K for $V_g = 2$V Between 100 K and 10 K all the resistances have a similar constant value of $R_{\square 1} \approx 1.6\ k\Omega \pm 50\ \Omega$, independent of V_g.

Between 10 K and 4.2 K, all the resistances slightly increase. The behavior of the sheet resistance when a back gate is applied is related to modifications of the mobility and of the electron density with the temperature. It can be associated to various scattering mechanisms and a freezing of the dopants that will not be analyzed in detail in this paper [5]. Whatever is the back gate voltage, the resistances vary weakly in the whole range of temperature showing no sign of divergence below 10 K

3.3 Magnetoresistance at very low temperatures

In order to investigate the ability of the material for quantum device operation, we measured the resistance at very low temperatures (10 mK < T < 1 K) using a dilution fridge Fig. 4 presents the sheet resistance as a function of the temperature. A significant increase of $R_{\square}$ up to 34 kΩ is observed below 1 K Fig 5 shows a typical magnetoresistance curve obtained at 400 mK. The measurements were carried out using a four-terminal scheme associated to a standard lock-in technique at 77 Hz, with low bias currents (10 pA - 1 nA) in order to avoid heating effects.

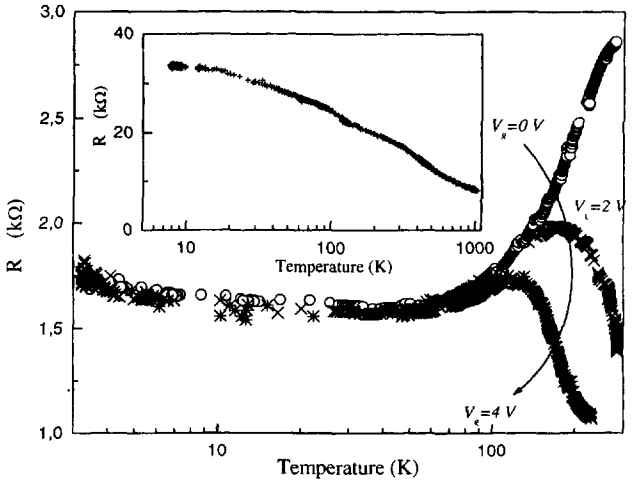

Figure 3 Temperature dependence between 300 K and 4 K of the resistance measured in 2 μm × 2 μm SOI-based van der Pauw, and for back gate voltages between 0 and 4 V The inset shows the resistance of the same structure measured between 10 mK and 900 mK

In the whole temperature range, a negative magnetoresistance is first observed at very low magnetic fields (B < 300 G), followed by a weaker dependence for 1900 G> B> 300 G Above 1900 G, R remains constant

4. DISCUSSION

The continuous increase observed in $R_{\square}$ at very low temperatures can be attributed to electron-electron interactions and quantum interference phenomena that are usually observed in low dimensional conductors [6]. This assumption is confirmed by the magnetoresistance. The observed behavior is characteristic of weak localization which is caused by the interference of time-reversed electron trajectories [7].

In the range of magnetic field 300 G < B < 1900 G, the magnetoresistance can be well described by the standard 2D weak localization theory, using the electron phase coherence length l_ϕ as the only adjustable parameter. This enabled us to evaluate l_ϕ as a function of temperature l_ϕ is found to be 90 nm at 800 mK, and increases up to 140 nm at 20 mK. This point will be discussed in details elsewhere

The amplitude and the shape and the low field peak (B < 300 G) could not be described by the standard weak localization theory. The amplitude of the peak is strongly temperature dependent For this range of magnetic fields, it can be possibly attributed to quantum interference effects This observation needs to be clarified in the future

The transition to a constant value in the magnetoresistance above 1900 G can be explained by a suppression of the weak localization corrections to the conductivity at $l_m = l$ [8], where $l_m = \sqrt{\hbar / eB}$ is the magnetic length, and l is the elastic mean free path According to this observation, we evaluated the mean free path $l \approx 60$ nm.

The constant value observed in $R_{\square}$(T) between 10 K and 100 K can be explained by the classical Drude model for conductivity in two dimensions [8]:

$$\sigma = en_s\mu = \frac{e^2 n_s \tau}{m^*} = \frac{2e^2 k_f l}{h} \qquad (2)$$

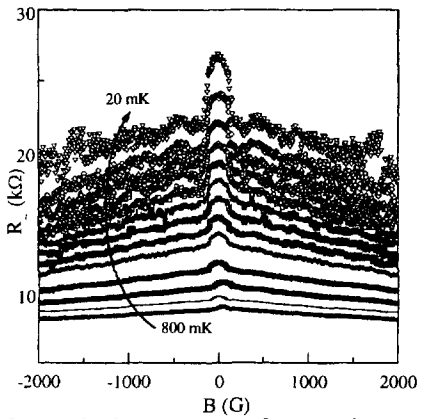

Figure 4: Longitudinal resistance as a function of magnetic field measured in a 2μmx2μm SOI-based van der Pauw, and for temperatures 20, 50, 100, 150, 200, 250, 300, 350, 400, 450, 500, 600, 700, and 800mK

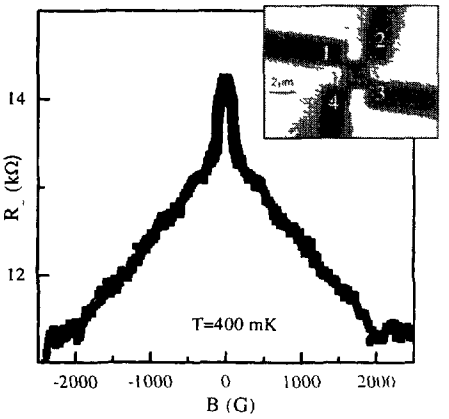

Figure 5: Magnetoresistance measured at 400 mK and between -2500 G and 2500 G The inset shows a SEM photograph of the structure

τ is the elastic relaxation time, n_s is the electron concentration, μ is the electron mobility, m^* is the electron effective mass, and k_f is the Fermi wave vector. In the last equation, we have used the identity $n_s = k_f^2/\pi$ [8]. Assuming that the system is two-dimensional, the sheet resistance was directly related to the conductivity $R = 1/\sigma$. Thus, we obtained an estimation of $k_f \approx 2.7\times10^8$ m^{-1}, $n_s \approx 2.3\times 10^{12}$ cm^{-2}, and $\mu \approx 1700$ cm^{-2}/V.s. The values deduced for the mobility and the mean free path are particularly high for such a structure, revealing a good quality material with few impurities. Such results would provide useful information for the implementation of SOI-based quantum devices

5. CONCLUSION

Electron transport properties of ultra-thin SOI nanostructures with van der Pauw geometry having 2 μm radius have been studied. The sheet resistance $R_{\square}$ was first measured at room temperature, and its dependence with the temperature was analyzed between 300 K and 4.2 K. Magnetotransport experiments were then performed at very low temperatures (10 mK - 900 mK) using a dilution fridge The experimental curves exhibit a negative magnetoresistance that can be explained in terms of quantum interference of electrons due to weak localization. An appropriate analysis of the results enabled us to evaluate for the first time the electron phase coherence length l_ϕ, the elastic mean free path l, and the mobility μ of the material at very low temperatures. The understanding of the fundamental properties of ultra-thin SOI layers is essential for the realization of nanoelectronics devices such as single electron transistors, and the results obtained in this work could be a first step towards new SOI-based quantum devices.

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