Lift-off lithography using an atomic force microscope

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We present a technique to fabricate nanostructures with an atomic force microscope (AFM). By taking advantage of the AFM tip sharpness, we engrave a narrow furrow in a soft polyimide layer. The furrow is then transferred using dry etching to a thin germanium layer which forms a suspended mask. Metallic layers are then evaporated through this mask. Metallic lines with a 40 nm linewidth and single-electron transistors have been fabricated. This lift-off technique can be used on any substrate and allows easy alignment with previously fabricated structures. © *1996 American Institute of Physics.* [S0003-6951(96)00846-7]

The observation of conductance quantization,[1,2] the controlled transfer of single electrons,[3] and the realization of almost perfect two-dimensional atoms[4] are recent examples of experiments involving nanostructures. Such results could be obtained because electron-beam lithography (EBL) has made sub-100 nm scale fabrication easily accessible. Although high-energy EBL reaches a resolution better than 10 nm,[5] there is a need for simple fabrication techniques in the sub-50 nm range. The atomic resolution imaging achieved by proximal probe microscopy has risen hopes that such alternatives to EBL do exist. Indeed, a variety of techniques have been developed,[6] culminating with the direct manipulation of atoms[7] and molecules.[8] Most of these techniques take advantage of the spatial resolution of the electronic emission from a tip to locally expose ultrathin electron resists,[9] such as self-assembled molecular monolayers[10] or Langmuir–Blodgett films,[11] or to directly modify the structure of the superficial layer,[12] such as the oxidation of hydrogenated silicon.[13] A few methods based on mechanically engraving a soft layer with a sharp atomic force microscope (AFM) tip have also been proposed.[14] In particular the PMMA resist bilayer process, commonly used in EBL, has been directly adapted.[15] We demonstrate in this paper the adaptation of the (PMMA/MAA[16]-Ge-PMMA) trilayer process,[17] in which the intermediate germanium layer forms a suspended mask. The main advantage of this process is to provide a rigid mask allowing large free-standing areas. The combination of multiple angle evaporations of various metals required to fabricate nanostructures combining narrow wires, small contacts, tunnel junctions or other elements, is then possible. We illustrate the versatility of the technique by fabricating a single-electron transistor (SET) aligned with previously deposited contacts. We have operated at low temperature and characterized this basic circuit of single electronics.

In the usual trilayer process, the pattern, created by e-beam exposure in the top PMMA layer, is transferred using dry etching to the intermediate metallic layer to form a suspended mask; further dry etching of the bottom layer provides the necessary undercut for proper lift-off after evaporation of metallic layers through the mask apertures. In the present process, depicted in Fig. 1, the top resist is replaced by a soft polyimide layer in which an AFM tip engraves a pattern of narrow furrows. Subsequent dry-etching steps are similar.

We first pattern on an oxidized silicon wafer the gold contacting circuitry by optical lithography. A gold thickness larger than 10 nm ensures that the contacting pattern is observable by scanning the sample surface with the AFM prior to engraving it, thus allowing easy alignment. This thickness should however be less than 50 nm in order to avoid large steps and ripples on the sample surface. A PMMA-MAA copolymer buffer layer with a thickness equal to the desired height for the suspended mask (200–300 nm) is then spun and baked. A germanium layer with a thickness in the 5–15 nm range is then thermally evaporated on top. At this stage, the wafer is diced, after which each chip is processed separately. Prior to engraving a chip, a thin polyimide layer with a thickness in the 15–20 nm range is deposited. Such a thickness insures that the furrows are deep enough to transfer the pattern properly during the subsequent dry-etching steps. Thin polyimide layers are obtained by spinning a highly diluted solution of polyimide (Dupont PI-2610) in N-methyl-2-pyrrolidinone (NMP). The solvent is removed by drying the chip on a hot plate at 60 °C. The chip is then placed in an AFM equipped with a rigid and sharp silicon tip (L=125

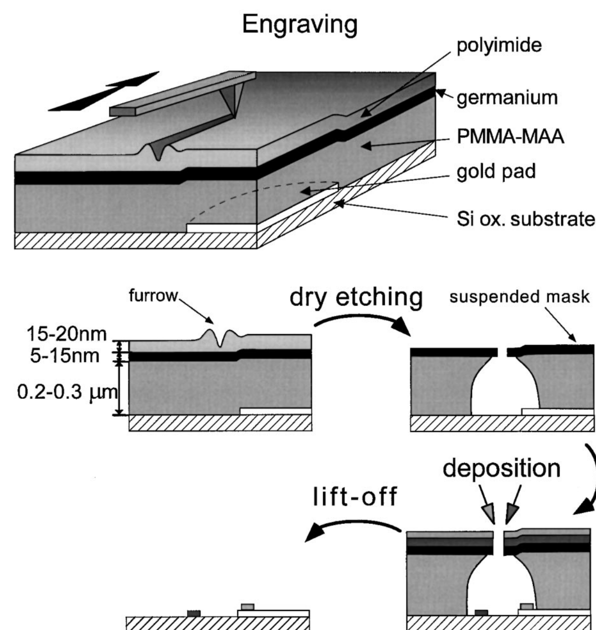

FIG. 1. Main steps of the AFM-based trilayer process.

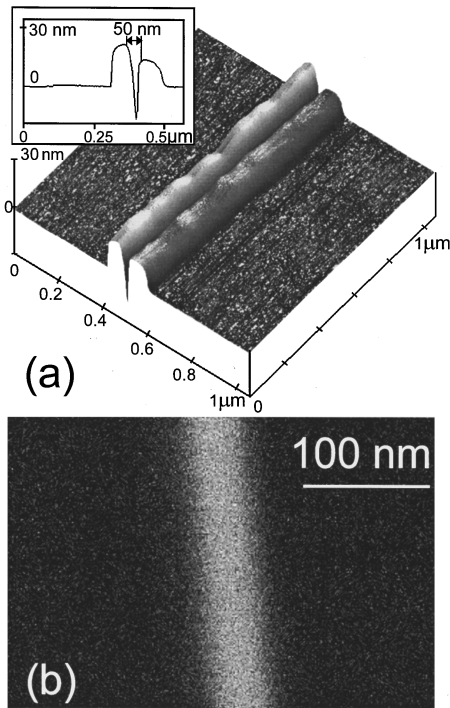

FIG. 2. (a) AFM image of a furrow engraved in polyimide. Note that the profile shown in inset, obtained by scanning with the scribing tip is somewhat broadened by the finite tip radius. (b) Scanning electron micrograph after deposition of 30 nm of gold through the corresponding mask.

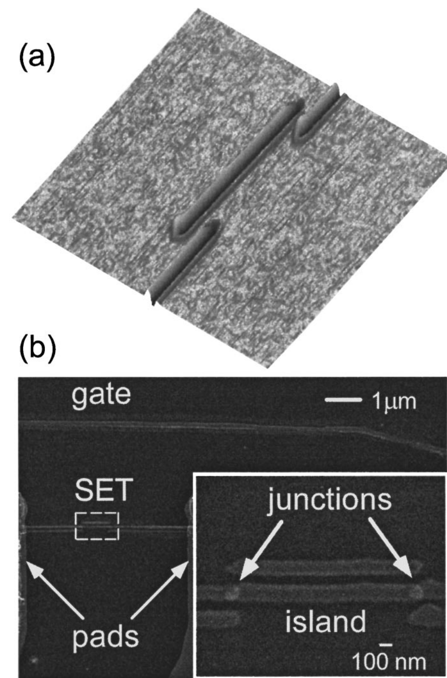

FIG. 3. (a) AFM image of the pattern engraved in polyimide for fabricating a SET. (b) Scanning electron micrograph of the SET device after fabrication.

μm, $k \approx 5\ \mathrm{N\,m^{-1}}$ from nanoprobe). The top surface is imaged to allow a precise alignment with the underlying pattern. Engraving is done by pushing the tip (see Fig. 1) at a velocity in the 0.2–2 $\mu\mathrm{m\,s^{-1}}$ range with an applied vertical force in the 1.5–3 μN range, higher speeds requiring larger forces.

One should take care not to scratch the solid Ge mask in order to preserve the tip sharpness. An AFM image of a typical 50-nm-wide furrow taken with the same tip as for engraving is shown in Fig. 2(a). It displays a constant profile without any irregularity in the edges: polyimide appears to be a well-suited material for engraving. Such a regularity is however not found if the tip is pulled, or pushed at angles exceeding 40° with respect to the cantilever axis, due to cantilever torsion by the asymmetric drag force. The obtained furrow profile is determined by the tip sharpness close to its apex, which is the main present limitation to the final line width. Fine control of the gap between two furrow ends [see Fig. 3(a)] is required to fabricate tunnel junctions by evaporating at two angles through the suspended mask. Small positioning corrections need to be applied in this case in order to compensate the cantilever flection under the effect of the applied force and of the drag force. Furrows up to 500 nm wide can be obtained by laterally sweeping the tip while pushing it.

The reactive ion etching (RIE) of the engraved chip is then done in three steps. A first etching is performed in a low-pressure (0.002 mb) SF_6 plasma in order to transfer the furrow to the Ge layer. The etching rate ratio between PI and Ge measured by laser interferometry is equal to 0.3, which allows a reasonable latitude in the adjustment of the etching time. The second and third RIE steps are done in an O_2 plasma, at respectively low (0.002 mb) and high (0.11 mb) pressures. The low-pressure RIE leads to anisotropic etching of the PMMA-MAA ballast down to the substrate. The high-pressure RIE provides isotropic etching and creates the undercut required for the angle evaporations. It is worth noticing that the transfer of the furrow pattern onto the Ge mask is realized without significant broadening.

We then proceed to the angle evaporation of one or several metallic layers through the suspended mask in an electron-gun evaporator. Tunnel junctions are obtained by *in situ* oxidation of an aluminum electrode prior to the deposition at a different angle of a counter-electrode. The height-width aspect ratio of the deposited lines is only limited by the obstruction of the mask due to the evaporated materials sticking on the mask edges. Finally, the Ge mask and the ballast are lifted off in hot acetone.

Figure 2(b) displays a scanning electron micrograph of a gold line deposited after etching the furrow shown in Fig. 2(a). The line is very regular with a 40 nm linewidth. Electrical continuity has been checked on 50-μm-long Al lines connected to 50-nm-thick gold pads.

Combination of evaporations at different angles allows one to fabricate various types of devices. In order to illustrate the versatility of the technique, we have fabricated single-electron transistors (SET) which are the basic circuits of single electronics. A SET consists of two nonsuperconducting tunnel junctions in series, with a small intermediate electrode (island) capacitively coupled to a gate electrode.[3] At temperatures such that $k_B T \ll E_c = e^2/2C$, where e is the electron charge and C the total island capacitance, the current flowing through the device is periodically modulated by the gate voltage V_g. The period corresponds to one extra electron charge induced on the island by V_g.

Both the device and the gate electrode have been fabri-

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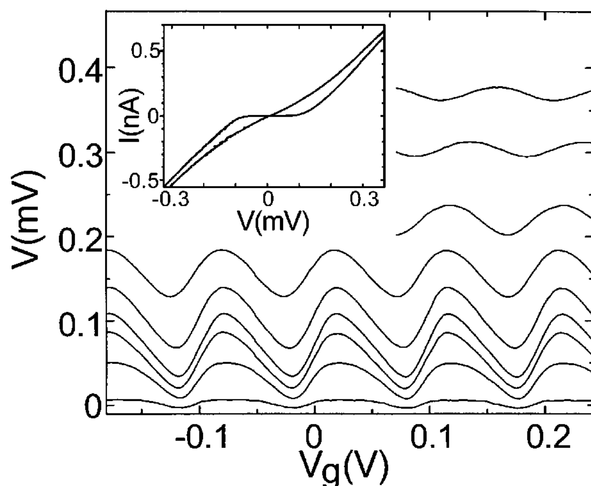

FIG. 4. Modulation curves of the output voltage V of the SET at 20 mK as a function of the gate voltage V_g for different bias currents. Inset: Extremal $I-V$ characteristics of the SET.

cated using AFM lithography. The AFM image of an engraved pattern and the scanning electron micrograph of the resulting SET are shown in Fig. 3. The two overlapping Al/AlO_x/Cu tunnel junctions have been obtained by two angle ($\pm 15°$) evaporations of Al and Cu. A series of $V - V_g$ modulation curves obtained at 30 mK are shown in Fig. 4. The charging energy E_c/k_B deduced from the $I-V$ is equal to 0.7 K. The device characteristics are completely similar to those of SETs fabricated using EBL.[3] AFM lithography has the advantage of avoiding deterioration of fragile underlying structures by e-beam exposure. In particular, defects in 2D electron gases have been reported to be a consequence of the EBL exposure.

In conclusion, the AFM-based trilayer lift-off technique presented in this work is a general purpose nanofabrication technique with alignment capability. It already offers an alternative to standard electron beam lithography in specific cases. Further progress in the tip sharpness could bring the linewidth under the presently achieved value of 40 nm.

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