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Nanometer scale patterning by scanning tunelling microscope assisted chemical vapour deposition

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Abstract

Single electron devices are of great interest for their possible replacement of transistors in memories. The key to the preparation of these components is the production of low capacitance dots, which requires a lithography step at nanometric scale. Direct patterning of metallic features at nanometric scale is possible by local decomposition of gaseous molecules under a scanning tunneling microscope (STM) tip, by application of a voltage of a few volts on the sample (STM assisted chemical vapour deposition). The gaseous molecules are dissociated by the high electric field (about 10^7 V/cm) within the tip–sample gap. Rhodium lines and dots have been deposited on gold or silicon surfaces by decomposition of $[Rh(PF_3)_2Cl]_2$. The influence of the sample voltage was studied and the resolution limit of the technique was investigated.

Keywords: Lithography; Single electron device; Chemical vapour deposition; Scanning tunneling microscope; Metallization

1. Introduction

It is planned that integration in ICs will double every 18 months, relying on an exponential rate decrease in MOSFET dimensions. However, it is generally believed that integration will stop when the MOSFET critical size (canal length) has decreased down to 30 nm [1].

Another problem posed by integration is the power consumption in ICs. In fact, it is well known that the transfer of 10^4–10^5 electrons is necessary for MOSFET commutation due to charge evacuation in junctions. This minimum current flow cannot be reduced and corresponds to a current density of 1.6–16 A/mm^2, assuming that the MOSFET commutation time is 1 ns and the wire section is 1×1 μm^2.

Single electron transistors (SET), based on the Coulomb blockade phenomenon, are now considered potential candidates to replace FETs in ICs. All these devices present identical features and

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are composed of low capacitance metallic or semiconductor islands separated from the other parts of the circuit by tunnel junctions [2,3]. In order to avoid spontaneous electron transfer in or out of the island, the charge energy of the islands must be much higher than the thermal agitation of the electrons ($K_B T \ll e^2/2C$), which leads to a condition on the island capacitance C and consequently on its size, which must not exceed 3 nm in order to obtain a device that will work at room temperature [2,3]. Such a resolution cannot be reached by the conventional lithographic techniques commonly used in the microelectronics industry (UV or e-beam) and, consequently, it is necessary to design new lithographic tools, based on new microscopy techniques to obtain resolution on the nanometric scale.

Proximal probes, i.e. AFM (atomic force microscope), STM (scanning tunnelling microscope) or SNOM (scanning near field optical microscope), have been used in different ways for direct patterning on suitably prepared surfaces, including oxide mask generation on a hydrogenated silicon surface [4–7] or direct writing of metallic features by local SPM (scanning probe microscope) assisted CVD (chemical vapour deposition) [8,9].

In the present work, noble metal (rhodium) nanofeatures were produced by STM assisted CVD from the dissociation of $[Rh(PF_3)_2Cl]_2$ molecules. The deposition process was investigated on gold and silicon surfaces. Dots and lines were drawn directly on the substrate and the resolution limit of the process determined.

2. Experimental setup and procedure

The experimental setup has been presented in a previous paper [10]. Briefly, the STM is placed inside a stainless steel chemical chamber. The base pressure of 5×10^{-7} mbar can be reached in a few hours by pumping with a turbomolecular pump, without baking the chamber. The chamber is mounted on a bulk steel plate insulated from low frequency vibrations by shock springs.

In order to perform electrical tests on the prepared nanodevices, these devices have to be linked to micron scale command electrodes previously drawn on the substrate surface. Due to the weak scan window of commonly marketed STM (about 8 μm), the STM tip has to be engaged on the substrate surface inside this test pattern with a precision of better than 4 μm. Consequently, an optical microscope with three magnifications (×2.5, ×5 and ×10), coupled to a video camera, has been fitted to the chamber and allows the observation of both tip and substrate during the tip engagement step. The substrate is placed on X–Y inertial piezo stages which allow precise substrate positioning just below the STM tip before initiating the tip engagement process. Fig. 1 shows a silicon substrate containing a gold test pattern observed using the optical system fitted to our STM equipment. The width of the gold lines converging from the large pads of the test pattern is 10 μm. The tungsten tip and its image (reflection on the substrate surface) can be seen.

The precursor is the inorganic molecule $[(PF_3)_2RhCl]_2$. It was prepared by the procedure described in the literature [11,12] adapted to a small amount of compound (typically 0.2 g of chloro(1,5-hexadiene) rhodium dimer reacted with PF_3 in pentane).

Experiments were performed in a static atmosphere of pure precursor. The gas pressure was varied in the range 10^{-4} to 10^{-2} mbar.

Deposition was performed on gold-coated mica substrates or on low-doped ($\rho = 5\ \Omega$ cm) n-type silicon (100) surfaces. Gold layers were produced by evaporation under vacuum at high temperature (400°C). This leads to atomically flat gold surfaces on areas as large as about 100×100 nm^2,

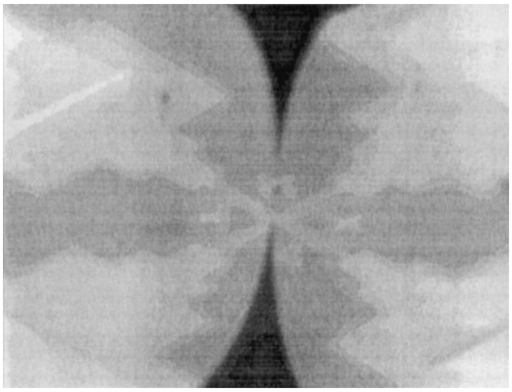


Fig. 1. Test pattern deposited on a silicon wafer observed with the optical microscope fitted to the STM equipment. Tungsten tips electrochemically prepared were used.

sufficiently flat to easily image the surface by STM and wide enough to perform local CVD on the nanometric scale [13].

During STM experiments, a bias is applied to the sample and a feedback loop maintains the tunnel current flow between the tip and the sample at a given setpoint value (typically 0.1–1 nA) while the tip is scanning the surface. Gold surfaces are typically imaged under 100 mV substrate bias and at a current setpoint of 300 pA. Under these conditions, the tip surface distance is about 0.5 nm [14]. Silicon surfaces are imaged under a substrate bias of 2 V.

Lithography of dots is performed by application of a pulse voltage on the substrate surface at a given position on the substrate leading to local decomposition of the molecules. In fact, because of the small tip–sample gap (about 0.5 nm) a pulse voltage of 3 V leads to a high electric field of 6×10^7 V/cm allowing decomposition of the molecule. In order to avoid tip surface contact while the rhodium dot is growing, the feedback loop of the STM is maintained during pulse voltage application. Moreover, since the current flow is fixed at the required setpoint value during deposition, to avoid tip removal when the voltage pulse is applied to the sample, the pulse duration has been chosen lower than the reaction time of the feedback loop of the STM (about 200 μs). Consequently, the electric field is constant during pulse application.

Tips are prepared by electrochemical etching of platinum or tungsten wires. This technique allows us to obtain very sharp STM tips (curvature radius about 5 nm) [15] avoiding multiple tip effects.

3. Results and discussion

3.1. The influence of tip voltage

Deposition of rhodium was only observed when negative pulses were applied to the sample in the presence of gas precursor, above a threshold of $|-2.7|$ V. Note that, under the same experimental conditions, no reaction is observed without precursor in the chemical chamber and, consequently, the deposited atoms originate from precursor decomposition and not from atomic transfer from the tip to the sample. Although the precursor is a rather symmetrical molecule [11,12] (symmetry roughly C2v), it should acquire a dipole moment when exposed to a strong electric field. Consequently, it seems that since the pulse polarity plays a role in the deposition process, the molecule is probably dissociated into several radicals during pulse application. One of these radicals containing a rhodium atom (or ion) has a positive charge and is attracted by the negatively biased surface.

3.2. Resolution of the lithographic technique

The resolution limit of the STM assisted CVD technique was studied on gold-coated mica surfaces. Multitunnel junctions consisting of a series of rhodium dots were prepared.

Fig. 2 shows the typical dimensions of the structures obtained. The dots were formed by application of 200 voltage pulses of $|-2.8|$ V at a frequency of 200 Hz on the substrate. The pulse duration was 200 μs. The dot diameter, measured by STM analyses, was 3 nm, while dot separation was found to be 4 nm. This series was produced in two steps. First, a lithography sequence was initiated to produce five dots. STM observation of the obtained structure showed that one dot was missing. Finally, a new lithographic sequence was initiated to add the missing dot, which demonstrates the precision of the method.

The resolution limit of this lithographic technique was investigated. In fact, dot size can be reduced by decreasing the number of voltage pulses applied to the sample. Fig. 3 shows two rhodium dots 1.9

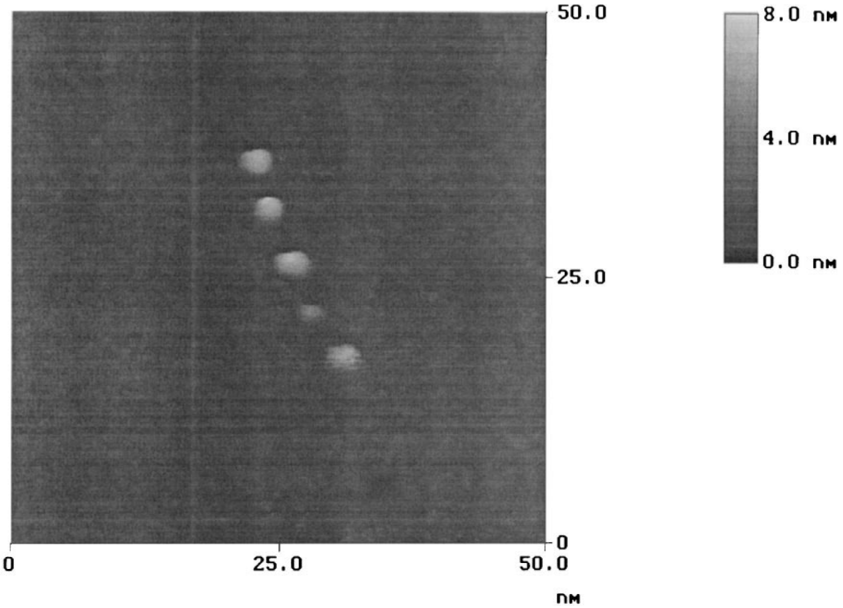


Fig. 2. Rhodium dots deposited on a gold-coated mica surface. The dots were obtained after 200 voltage pulses. The pulse duration was 200 μs and the voltage −2.7 V. The gas pressure was 5×10^{-3} mbar.

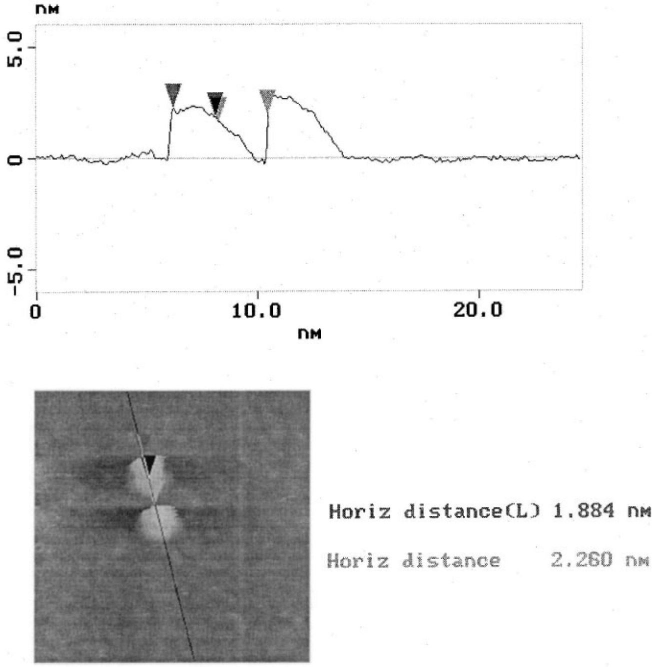


Fig. 3. Resolution limit of lithography by STM assisted CVD. Rhodium dots were deposited on a gold surface at a pressure of 5×10^{-3} mbar. Fifty voltage pulses of 200 μs were applied to the sample.

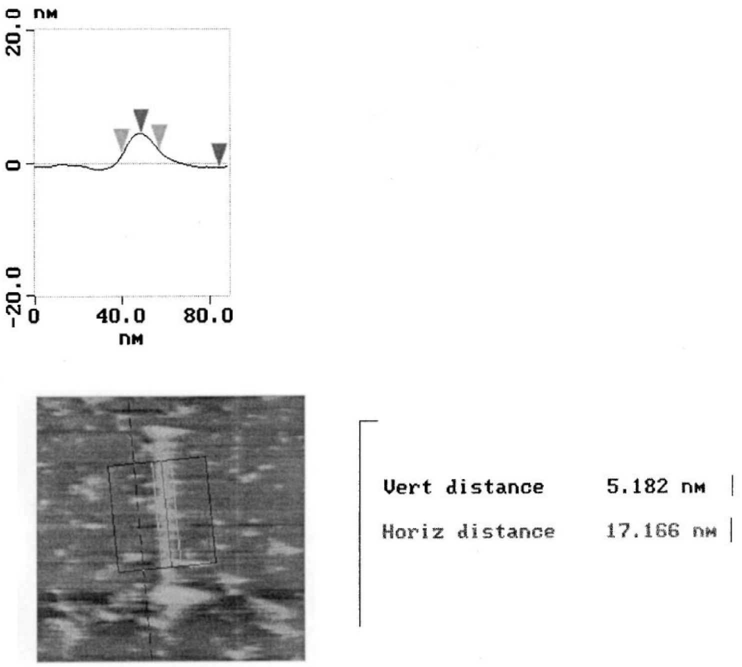
nm wide, spaced 2.3 nm apart. These dots were deposited on a gold surface by application of 50 voltage pulses of 200 μs under a gas pressure of 5×10^{-3} mbar.

3.3. Deposition on silicon surfaces

STM experiments require that we work on conductive substrates, consequently the native oxide layer has to be removed from the silicon surface before surface imaging. Surfaces are prepared by a RCA conventional wet etching process [16], which is known to passivate the surface by mono-atomic Si–H bonds which impede surface oxidation during air exposure. Lithography experiments were performed on these passivated surfaces.

No deposition was observed for both polarities. However, rhodium dots were successfully deposited by application of a sequence of positive voltage pulses at +6 V followed by negative voltage pulses at −2.8 V to the substrate. The fact that no deposition occurs, even for negative pulses, suggests that hydrogen passivation impedes rhodium cluster nucleation.

Studies on oxide mask pattern generation on hydrogenated silicon surfaces have shown that hydrogen can be locally removed from silicon surfaces by application of a negative bias on an AFM tip [4]. In our case, the positive voltage pulses previously applied to the silicon sample probably induces local hydrogen desorption which locally enhances the rhodium nucleation step and finally



Vert distance 5.182 nm

Horiz distance 17.166 nm

Fig. 4. Rhodium line deposited on a silicon surface. The line was obtained after 400 passages at a scan speed of 250 nm/s. The gas pressure was 5×10^{-3} mbar, while a voltage of -6 V was applied to the sample.

allows rhodium dot deposition. The value of the pulse voltage necessary to remove hydrogen from the passivated silicon surface is consistent with results found in the literature [17].

The resolution obtained on silicon surfaces is of the same order of magnitude as on gold surfaces.

3.4. Rhodium line deposition

The rhodium line deposition process was studied on a silicon surface. Fig. 4 shows the typical line characteristics obtained. This line was obtained after 400 passages at a scan speed of 250 nm/s and under a voltage of -6 V applied to the sample under a gas pressure of 5×10^{-3} mbar. The line contour is quite regular and the linewidth measured at half height is typically 17 nm, while the line height is about 5 nm. These dimensions are consistent with data found in the literature [18].

4. Conclusion

Rhodium features (lines or dots) have been successfully deposited on gold and low-doped silicon surfaces by local decomposition of $[Rh(PF_3)_2Cl]_2$ molecules under a STM tip when a few volts is applied to the sample. On gold surfaces, the reaction occurs only when negative voltages are applied to the sample above a threshold of $|-2.7|$ V.

On hydrogenated silicon surfaces, rhodium deposition is inhibited by the presence of hydrogen on the surface, which impedes rhodium nucleation. However, rhodium dots can be obtained above the same voltage threshold of $|-2.7|$ V, providing a series of positive voltage pulses (6 V) are applied to the sample in order to remove local hydrogen atoms from the surface.

Dots as small as 2 nm, spaced 2.3 nm apart, can easily be patterned directly by this technique, a resolution which cannot be attained using the conventional lithography technique.

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