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Physica E 13 (2002) 999–1002

PHYSICA E

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Electronic transport properties of single-crystal silicon nanowires fabricated using an atomic force microscope

N. Clément[a], D. Tonneau[a,*], H. Dallaporta[a], V. Bouchiat[a], D. Fraboulet[b], D. Mariole[b], J. Gautier[b], V. Safarov[a]

[a] *GPEC, Department de Physique, Faculté des Sciences de Luminy, Case 901, F-13288 Marseille Cedex 9, France*
[b] *LETI/DMEL, CEA-Grenoble, 17 av. des Martyrs, F-38054 Grenoble Cedex, France*

Abstract

We present electrical characterization of silicon nanowires made from ultrathin silicon-on-insulator (SOI) using a lithography process based on an atomic force microscope (AFM). SOI wafers were first thinned, prepatterned and doped using conventional microelectronics processes in order to elaborate contact leads and pads. Between contacts, the upper Si was further thinned down to 15 nm and n-doped by arsenic implantation. The Si top layer is then locally patterned using local oxidation induced under the biased tip of the AFM. The active part of the device is finally obtained by silicon selective wet etching using the AFM-made oxide pattern as a mask.

This technique was used to study electrical transport through silicon wires with sub-1000 nm^2 cross-section. The implementation of both side gates and backgate control allowed to test a full device which acts at room temperature as a field effect transistor. Current densities as high as 2×10^5 A/cm^2 can be switched off by lateral gate control. At low temperatures, aperiodic oscillations of the nanowire current are observed while the gate voltage is swept. This behavior is attributed to potential variations along the wire caused by random fluctuations of dopants. © 2002 Elsevier Science B.V. All rights reserved.

PACS: 85.30.Wx; 85.40.Hp; 85.40.Ux

Keywords: AFM; Lithography; Silicon-on-insulator; Silicon nanostructures

1. Introduction

Since the feasibility demonstration of oxide mask generation on a silicon wafer by a scanning tunneling microscope (STM) [1], a great amount of interest has been devoted to proximal probe-assisted lithography techniques [2]. This pioneer process was based on a local oxidation of silicon induced by application of a volatge on the STM tip which lead to a highly localized anodization mechanism. Atomic force microscope (AFM) is preferred to STM because the oxide layer formed just under the tip has no influence on the tip altitude control above the substrate [3,4]. This has already been used successfully by Campbell et al. [5] to design an elementary device, a lateral gate field effect transistor (FET) connected to its command electrodes. Their starting substrate was a SIMOX wafer with a 40–200 nm-thick silicon upper layer.

Using a method similar as presented in Ref. [5], we have tried to scale down the size of this component starting from ultrathin Unibond® SOI wafers [6] instead of SIMOX samples. In fact, the Smart-Cut® [7] fabrication step ensures the crystalline properties of

* Corresponding author. Fax: +04-91-82-91-76.
E-mail address: tonneau@gpec.univ-mrs.fr (D. Tonneau).

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PII: S1386-9477(02)00288-6

the silicon top-layer, even for ultra-thin silicon layers (thickness as low as 5–20 nm), and allows to obtain a very sharp interface silicon layer/buried oxide. The electrical conductance of silicon nanowires (section of $15\times50\ \text{nm}^2$) at room and low temperatures (4–15 K) elaborated by AFM lithography on these thinned SOI samples has been measured. The effect of lateral and backgate voltages on the wire electrical characteristics are presented and discussed.

2. Fabrication process

The principle of AFM lithography on a silicon wafer has already been described in the previous papers [1,3,4]. The (1 0 0) silicon wafer is previously passivated by dipping in a hydrogen fluoride solution (2% in water) during 1 min [8] treatment which is known to saturate the dangling bonds of the silicon surface by hydrogen atoms [9]. Hydrogen atoms can be locally removed with an AFM when a negative bias U_{tip} is applied. It leads to a local oxidation of the substrate via a field-enhanced oxidation process by anodization [10]. The oxidation reaction occurs only if U_{tip} is chosen higher than a threshold of -2.7 V [11,12].

The ambient humidity is kept constant at a level of 30–40%. Applying a tip voltage while the tip is scanned over the silicon surface at speed of 0.1–1 μm/s leads to an 0.2–2 nm-thick oxide pattern of width 20–60 nm. The oxide features formed by AFM lithography can be then transferred to the silicon wafer by a step of silicon wet etching, by tetramethyl-amino-hydroxide (TMAH) solutions. TMAH solution (25% in water) has been preferred to classical KOH for oxide mask transfer due to the high selectivity (2000:1) of the silicon etching kinetics with respect to SiO_2 etching. On SOI samples, this process allows to remove all the non-patterned areas down to the buried oxide, leading to silicon nanostructures supported on an insulating layer (Fig. 1).

As-doped Unibond ® silicon-on-insulator (SOI) samples with an ultra-thin single-crystal silicon top layer (typically 15–20 nm) were used. One advantage of this technology is that it ensures a very sharp interface top silicon layer–silicon dioxide (see inset of Fig. 1). In order to perform electrical tests on the elaborated nanostructures, a test pattern has previously been fabricated using conventional photolithography processes. This connection pattern is made of highly doped silicon obtained by phosphorous ion implantation and consists in 100 μm^2 contact pads connected to leads converging to the central working zone of the chip. This active area is thinned down to 15 nm by localized thinning process (LOCOS—series of oxidation/oxide stripping) and doped by arsenic ion implantation at 8 keV, with two different surface doses of respectively 5×10^{11} and $2\times10^{13}\ \text{cm}^{-2}$, followed by rapid thermal annealing at 950°C for 30 s. This leads to two different doping levels of roughly 2×10^{17} and $10^{19}\ \text{cm}^{-3}$, that will be referred, respectively, as mildly doped and heavily doped samples in the following.

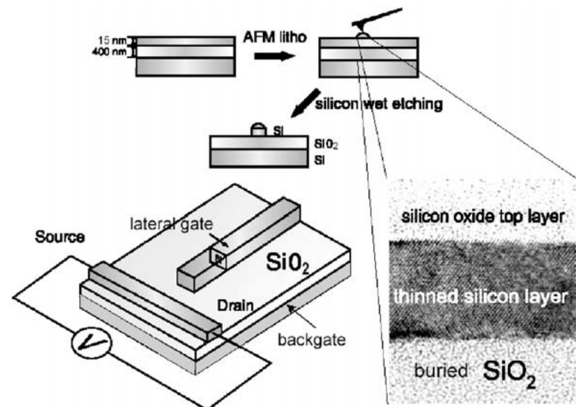

Fig. 1. Schematics of the process for silicon nanodevice fabrication involving an AFM lithography step. Inset: transmission electron micrograph of a thinned Unibond SOI substrate showing the good crystalline structure of the Si upper layer.

3. Electrical characterization

In order to track possible problems that can arise with this new process, we have decided to focus on devices with a very simple geometry: a silicon nanowire connected to two highly doped silicon pads acting, respectively, as source (S) and drain (D), with one or two side fingers approaching the nanowire and acting as coplanar lateral gates (see scheme in Fig. 1). The bulk Si below the buried oxide layer also acts as an extra gate, called backgate in the following. Low-roughness nanowires with a constant width of 50 nm are typically obtained, while the channel

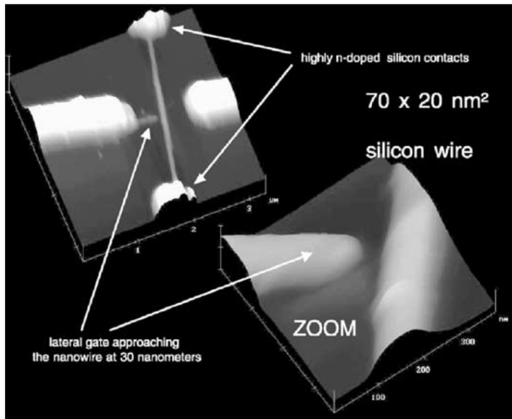

Fig. 2. AFM micrograph of a side-gated silicon nanowire acting as field effect transistor. The nanowire was doped at 2×10^{17} cm^{-3}.

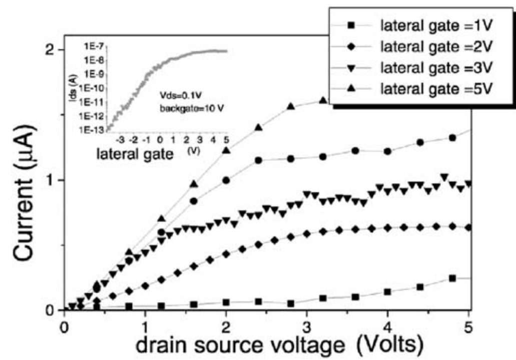

Fig. 3. I_{DS}–V_{DS} curves and I_{DS}–V_G transconductance (inset) curves acquired at 300 K for the silicon nanowire device presented in Fig. 2. A constant backgate of 10 V was applied.

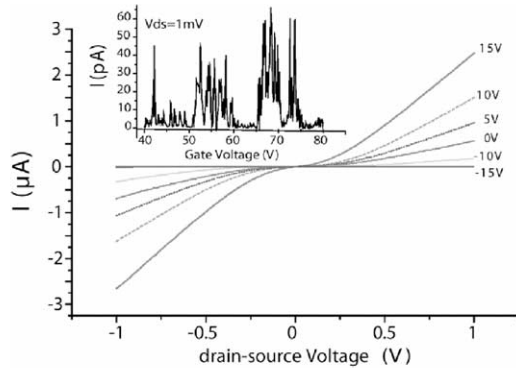

Fig. 4. I_{DS}–V_{DS} characteristics of the nanowire at low temperature (13 K) for different backgate voltages ranging from −15 to +15 V. Inset: nanowire current oscillations at a source–drain bias voltage of 1 mV as the backgate voltage is swept.

thickness is fixed by the silicon top layer of the starting SOI sample (15 nm) (Fig. 2). Thanks to the absence of proximity effect during lithography or etching, side gates can be approached at distances as low as 30 nm (see Fig. 2, zoom), without any noticeable current leakage.The device is then wire bonded and electrical properties are measured either in vacuum or in a dry, inert atmosphere (He).

Room temperature electrical characteristics of nanowires made from the heavily doped SOI shows for all tested devices a noiseless and reproducible ohmic behavior. The measured resistance correctly scales with the length over section ratio, except for the tiniest wires (with a cross-section below 600 nm^2) for which an increased effective resistivity is observed. The average resistivity of all heavily doped (10^{19} cm^{-3}) nanowires is found to be 83 mΩ cm, a value higher by a factor of 14 than expected from the design data of 6 mΩ cm (a factor of 7 for the largest wires). This discrepancy was already observed in silicon nanostructures [13,14]. It is attributed to a surface depletion effect which can be large in such structures due to the important surface/volume ratio which occurs in nanoscale silicon. On mildly doped samples, the wire is fully depleted. For example, on the device presented in Fig. 2, a voltage of 10 V has to be applied to the backgate to restore the ohmic behavior at low drain–source voltages (Fig. 3). At room temperature, a current density up to 2×10^5 A/cm^2 flows through the wire. It can be reduced by 5 orders of magnitude by a voltage variation of 4 V applied on the lateral gate (see inset Fig. 3). This Si nanowire, therefore, acts as a lateral gate nano-FET with a large gate transconductance gain.

At low temperature (4–13 K), for heavily doped nanowires, the transport is nonlinear and follows a thermally-activated behavior (Fig. 4). With a positive backgate voltage, the wire recovers an ohmic behavior at low drain–source voltages V_{DS}. Furthermore, it presents noise features as it is reported in other works for SOI nanowires made by electron beam lithography [5,13]. At 13 K and for low drain–source bias voltages (0.1–10 mV) the drain–source current presents oscillations with respect to the gate voltage. These

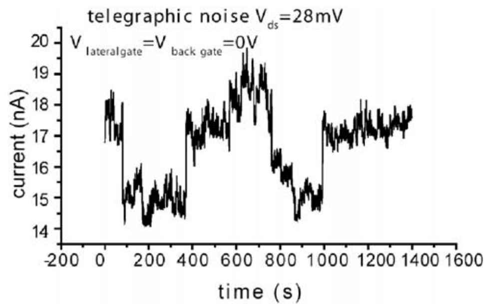

Fig. 5. Time trace of the nanowire drain–source current showing the telegraph switching behavior. It was acquired at 4 K with all gates grounded.

oscillations are found reproducible by scanning back and forth either the backgate or the sidegate. Due to a capacitance of the sidegate lower than the backgate capacitance, current oscillations span over a larger voltage range using the sidegate.

At lower temperatures (4 K) and at bias voltages V_{DS} lower than 5 mV, these oscillations change to aperiodic conduction peaks (see Fig. 4, inset) separated by a perfectly insulating behavior. They are attributed to the random distribution of dopants along the wire which is responsible for large potential fluctuations along the wire and leads to potential wells centered around dopants. They eventualy lead to a multiple tunnel junction configuration [13] and current peaks result from a percolation path between potential wells.

Further analysis of the drain–source current noise behavior shows that the current randomly switches in time between discrete levels (Fig. 5). These random telegraphic fluctuations were found to be as large as 50% of the total current flowing through the wire. Surface charges similar to those encountered in MOSFET gate oxide [15] cannot account for such a large fluctuations. It is more likely that these current fluctuations arise from thermally activated switching between two percolation paths.

4. Conclusion

AFM lithography has been used successfully on Unibond® SOI wafers to elaborate connected n-type silicon nanowires with a section of 50×15 nm^2 on insulator. The effects of gates on the wire transconductance have been investigated. At room temperature the device exhibits electrical characteristics similar to those of conventionnal FET, for high backgate voltage. At low temperature, the channel behavior is no more ohmic and insulating behavior is observed at low bias V_{DS} in I_{DS}–V_{DS} characteristics. Transconductance fluctuations are also observed at constant V_{DS} when the backgate voltage is varied.

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