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Integration of self-assembled carbon nanotube transistors: statistics and gate engineering at the wafer scale

L Marty[1,6], A Bonhomme[2], A Iaia[1], E André[2], E Rauwel[3], C Dubourdieu[3], A Toffoli[4], F Ducroquet[4,5], A M Bonnot[1] and V Bouchiat[2]

[1] Laboratoire d'Etudes des Propriétés Electroniques des Solides, CNRS-UJF, BP 166, Grenoble Cedex 9, France
[2] Centre de Recherches sur les Très Basses Températures, CNRS-UJF, BP 166, Grenoble Cedex 9, France
[3] Laboratoire des Matériaux et du Génie Physique, UMR CNRS 5628, ENSPG, Minatec, 3 parvis L Néel, BP 257, 38016 Grenoble Cedex 1, France
[4] CEA-LETI, 17 avenue des martyrs, 38054 Grenoble Cedex, France
[5] Institut de Microélectronique, Electromagnétisme et Photonique, UMR CNRS 5130, Minatec—INPG, BP 257, 38016 Grenoble Cedex 01, France

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Abstract
We present a full process based on chemical vapour deposition that allows fabrication and integration at the wafer scale of carbon-nanotube-based field effect transistors. We make a statistical analysis of the integration yield that allows assessment of the parameter fluctuations of the titanium–nanotube contact obtained by self-assembly. This procedure is applied to raw devices without post-process. Statistics at the wafer scale reveal the respective role of semiconducting and metallic connected nanotubes and show that connection yields up to 86% can be reached. For large scale device integration, our process has to implement both wafer-scale self-assembly of the nanotubes and high transistor performances. In order to address this last issue, a gate engineering process has been investigated. We present the improvements obtained using low and high κ dielectrics for the gate oxide.

1. Introduction

Field effect transistors based on carbon nanotubes (CNFETs) are the most promising devices emerging from the field of molecular electronics. Indeed CNFETs exhibit sufficient reproducibility, speediness, and high enough gain to behave as active components in logic circuits, leading to performing a digital function [1] that can operate at high frequency [2]. Their performances even exceed [3, 4] those obtained by state-of-the-art silicon MOSFETs.

However, numerous obstacles remain to be overcome, before seriously considering them in nanoelectronics. The two biggest challenges are firstly to realize a successful integration of these devices at the wafer scale and secondly to eliminate the device performance fluctuations arising from the lack of control of the nanotube diameter and chirality.

The critical step in CNFET integration is to implement at the same time many reliable metal/single nanotube electrical connections in parallel. This step requires massively parallel assembly methods that allow skipping the tedious alignment procedures that are incompatible with industrial applications.

Several technologies have shown progress in addressing the first issue. One can sort them into two categories. The first category consists of 'wet self-assembly' techniques that involve either chemical self-assembly based on surface [5, 6] or nanotube functionalization, DNA directed deposition [7] or dielectrophoresis [8]. The second category consists of *in situ* guided growth, mainly based on catalytic CVD methods [9]: they enable batch processing and provide the scalability required to open the way to practical applications. Trials

[6] Present address: Université de Montréal, 2900 E. Montpetit, Montréal, QC, H3T 1J4, Canada.

of massively parallel procedures to connect nanotubes [9–12] and semiconducting nanowires [13] in parallel without the need of individually monitored nanopositioning have provided significant advances.

There is a lack of information about the average yield for most of these assembly techniques. However, the possibility to obtain batches of integrated devices [14, 15] allows the statistical investigation of their electronic properties and the determination of a reproducible yield that can be reliably correlated with the fabrication parameters. It is then possible to get quantitative results on the dispersion of key parameters, a mandatory step towards the validation of upscaling capability.

Following this idea, we present in this paper a statistical wafer-scale characterization of self-welded carbon nanotube field effect transistors fabricated using a parallel integration chemical vapour deposition-based (CVD) process. We extract general trends from the electrical statistics obtained on batches of self-connected devices. By analysing the resistance and switching performances of a given batch of CNFETs, we show that it is possible to characterize the process in terms of connection yield for both semiconducting and metallic nanotubes. Moreover, we propose technological issues involving new gate dielectrics to improve the device characteristics.

2. Experimental details

Carbon nanotubes (CNTs) have been synthesized by the hot filament assisted chemical vapour deposition (HFCVD) technique [16]. Such a technique provides simultaneous self-welding and localized growth of nanotubes by controlling the catalyst location. Electrodes were pre-patterned on an oxidized silicon substrate (1 μm thick oxide) by deep UV lithography to obtain sub-micron-wide gaps between them. We then performed evaporation and lift-off of a 30 nm thick layer of titanium covered with a thin 0.5–2 nm Co catalyst film. HFCVD was then directly performed. The vapour was composed of methane strongly diluted in hydrogen (5–20 vol%). During the synthesis, a tungsten filament placed at 1 cm above the substrate holder was heated up to 1900–2100 °C, while controlling the deposition temperature with an additional heater placed in the substrate holder. Typical deposition temperatures were in the 750–850 °C range.

During the HFCVD step, CNTs grow directly from one catalyst-covered electrode and connect the facing one [17]. As the electrical connection is performed *in situ*, the devices are operational right after the growth and without any post-process. This allows us to test the transparency of the as-grown titanium/nanotube interface, which is known to provide reliable contacts [18]. Moreover, this process is scalable up to wafer-scale integration with a good yield, which is here demonstrated using 2 inch diameter wafers with about 9000 pre-patterned electrode pairs.

Electrical measurements are performed on two batches (denoted A and B) corresponding to different growth parameters. Details of the growth conditions are similar to what is presented in previous studies [19]. While all other parameters were kept constant, the methane proportion in the chamber was decreased by 0.4% for wafer B compared to A, leading to respectively high and low growth yields for samples A and B.

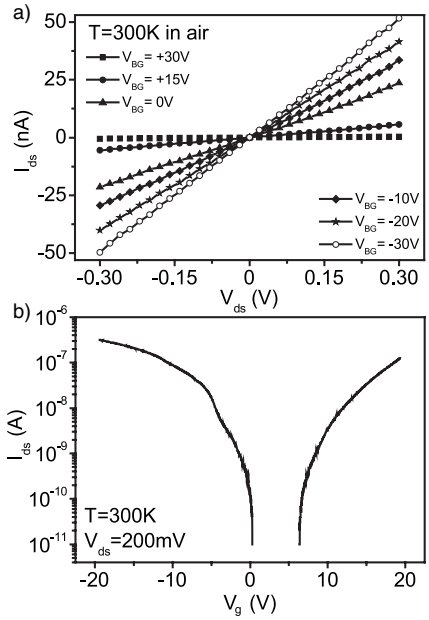

Figure 1. (a) Drain–source I–V characteristics of a standard unipolar p-type device (wafer A) at 300 K in air for different back-gate voltages. (b) Transfer characteristics at 300 K in vacuum for a typical back-gated ambipolar device (wafer A).

3. Results and discussion

Conductance of the devices was measured in an automatic probe station using a constant drain–source voltage V_{ds} = 100 mV, while the p-doped silicon substrate was used as the back gate. Our fabrication process leads to both p-type and ambipolar as-grown CNFETs [20]. The I–V curves of a unipolar p-type CNFET and the backgate transfer characteristics of a typical ambipolar CNFET device are plotted in figure 1. A convenient way to characterize the dispersion of FET performance is to plot the current in the *on*-state (in our case for a back gate of $\pm$30 V) with respect to the current in the *off*-state (typically with a grounded back gate).

Figure 2 shows such a plot gathering data obtained from conductance measurements of 203 devices regularly distributed over wafer A, which gives a statistical uncertainty of $\frac{1}{\sqrt{203}} = 7\%$. We plotted the statistical histogram considering the *on*-state current ratio I_{on}/I_{off}. Multiple features are revealed by these statistics.

First, we measured a significant *on*-state current for 86% of the devices, which shows the efficiency of this technique to connect carbon nanotubes *in situ*. The non-connected devices (NC) appear at $I_{ds} = 10^{-12}$ A, which corresponds to the resolution limit of the measurement unit. We distinguish three different types of device among the connected ones (as shown by the ellipses in figure 1(a)). The first group of devices corresponds to the less resistive circuits, which also do not exhibit any field effect ($I_{on} = I_{off}$, diagonal of the diagram). These data correspond to devices having a well connected metallic nanotube dominating the transport. They represent 24% of the 203 tested devices (figure 1(b)), which corresponds to 28% of the connected devices. For all other devices, the *on*-state conductance is significantly lower and

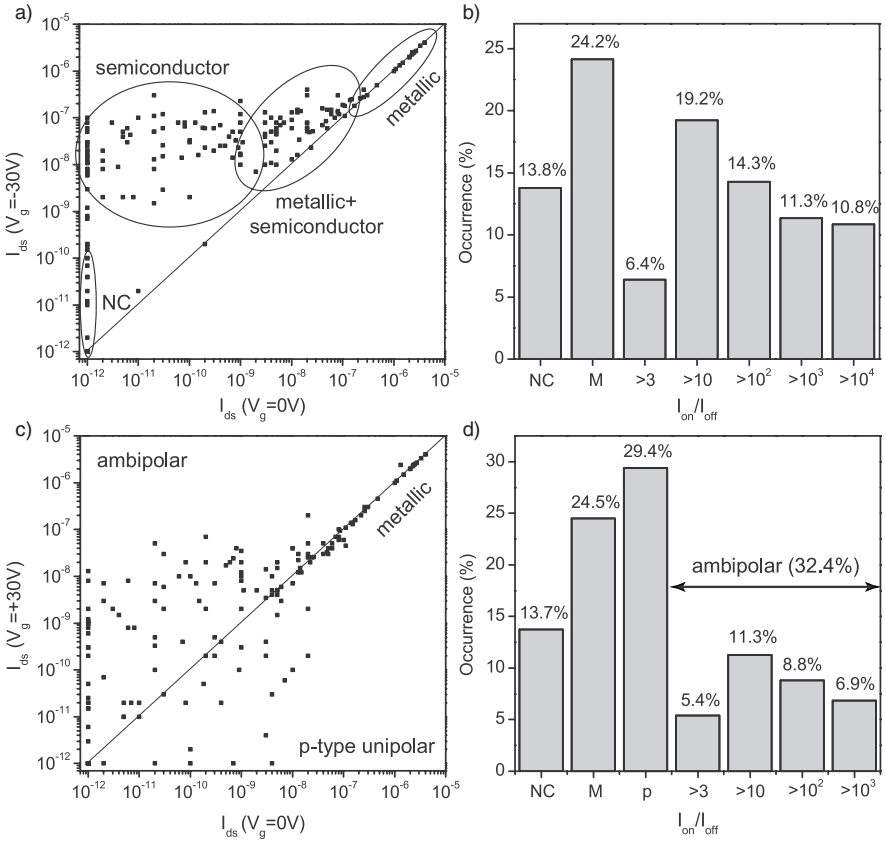

Figure 2. Statistics on CNFETs distributed over a high yield CNFET wafer (wafer A). (a) Statistics for the p branch: the current in the p branch *on*-state ($V_g = -30$ V) is plotted versus the current in the *off*-state ($V_g = 0$ V). The drain–source voltage is set at $V_{ds} = 100$ mV. The line is the frontier where both currents are equal. Each point corresponds to a single device on the wafer. The line obtained at 10^{-12} A corresponds to the detection limit of the set-up. (b) The statistics of (a) are plotted as a histogram versus the rate I_{on}/I_{off}. NC corresponds to the non-connected devices and M to the one having no field effect and thus a metallic behaviour. (c), (d) The same graphs for the n branch ($V_g = +30$ V). The 'p' bar on the histogram corresponds to the circuits having $I_{on}/I_{off} < 1$ and thus a p-type unipolar behaviour.

a field effect is observed. A second group of devices can be extracted (ellipse in the upper central part of figure 2), corresponding to the intermediate gate modulation and device conductance, which is attributed to semiconducting nanotubes connected in parallel with metallic ones that short the circuit in its *off* state. Finally, the left ellipse corresponds to the most resistive devices, exhibiting several orders of magnitude of current modulation. This last group is thus associated with fully semiconducting devices. 22% of the total devices exhibited at least 10^3 for their I_{on}/I_{off} ratio, a performance suitable for logic gate applications [1, 21].

The situation is totally different for the field effect exhibited at positive gate voltages (i.e. the n branch). Usually, CNFETs exposed to ambient air are unipolar p-type transistors, due to the modification of the Schottky contact barriers by adsorbed oxygen [22]. However, it is possible to get stable n-type and even ambipolar CNFETs by adapting the contact barriers with an annealing followed by a protective encapsulation [22] or using an appropriate metal for the electrodes [23]. In contrast with usual CNFETs, our fabrication process leads to air-stable ambipolar transistors, probably because of the presence of small bandgap semiconducting nanotubes such as double wall nanotubes (DWNTs) as reported previously. The field effect for the n branch shown in figures 2(c) and 4(c) shows a different behaviour. Although we find the same number of non-connected and metallic devices as for the p branch, half of them exhibit an I_{on}/I_{off} ratio higher than unity and the ratio for the other half is lower than unity at $V_g = +30$ V. This identifies two kinds of CNFETs: the ambipolar ones exhibiting a field effect for positive gate voltages too, and the p-type unipolar ones, which are even more blocked at positive gate voltages than at $V_g = 0$ V. Transmission electron microscopy on nanotubes [24] revealed that this growth technique can provide in the same batch single and double walled carbon nanotubes. We attribute the existence of both unipolar and ambipolar devices to the presence of both types of nanotubes [25].

Moreover, clear correlations between the conductance of the devices and the amplitude of the field effect appear in figure 3. The graphs represent the *off* state resistance (a) and the *on* state one (b) versus the I_{on}/I_{off} ratio for the p branch. First, the low resistive devices (average conductance $G^0_{metal} = 5 \times 10^{-5}$ S) correspond to the points at $I_{on}/I_{off} = 1$ as they exhibit no field effect, which has been ascribed previously to at least one well coupled metallic nanotube. Other devices exhibit a field effect and have a mean *on*-state conductance $G^0_{on} = 10^{-6}$ S, which is remarkably independent of the I_{on}/I_{off} ratio. This means that the *on* state of a semiconducting device is

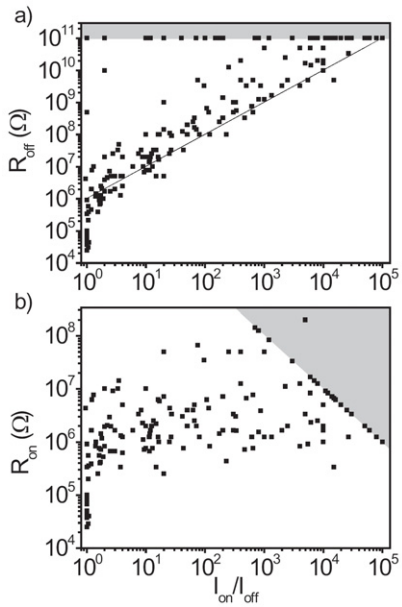

Figure 3. (a) Resistance in the off state plotted versus the on-to-off current ratio for wafer A. The line corresponds to the calculated R_{off} with our model. (b) The same for resistance in the on state. In both cases, the grey zone corresponds to the detection limit of the set-up.

scarcely affected by the nature and the number of the nanotubes connected in parallel, while the off state critically depends on the occurrence and quality of the metallic nanotube contact.

From SEM imaging, we estimate the number of connected nanotubes ranging between one and ten per device. Assuming an on-state conductance of $G^0_{on} = 5 \times 10^{-7}$ S per single semiconducting nanotube, this gives a range of conductance of one decade: 0.5–5 μS, which is a good agreement with the statistical dispersion of conductance observed in figure 3(b). Due to the high temperature used for the self-assembled titanium/nanotube contact, we believe that the conductance fluctuations are dominated by the number of connected nanotubes. However, more detailed studies of the conductance distribution curves are required to fully separate the respective influence of the contact conductance fluctuations from those arising from the fluctuation of the number of connected nanotubes.

One notes also that the *off*-state conductance decreases linearly with the I_{on}/I_{off} ratio. This second behaviour can be explained by considering a simple model taking into account the mixed contributions of both metallic and semiconducting nanotubes connected in parallel. Indeed, the total conductance G of a given device can be written as a sum over the metallic nanotubes (with individual conductances G_i) and the semiconducting nanotubes (with individual conductances $G_i(V_g)$:

$$G(V_g) = \sum_{\text{metal}} G_i + \sum_{\text{semi}} G_j(V_g).$$

Considering the devices having a significant field effect, it appears clear that the semiconducting nanotubes dominate the conductance in the *on* state (p branch). If this were not the case, the field effect would be entirely masked by the metallic shunts. Similarly, only the metallic nanotubes contribute in the *off* state, therefore the previous relation giving the device conductance can be drastically simplified for it maximum and minimum values: $G(-30\ \text{V}) \approx \sum_{\text{semi}} G_{on}$ and $G(0\ \text{V}) = \sum_{\text{metal}} G_i$. Such a discriminating effect has been successfully used to protect semiconducting nanotubes during breakdown of metallic ones by a high voltage [26]. This allowed selective destruction of the metallic nanotubes while keeping the semiconducting ones unaffected and led to increasing the CNFET I_{on}/I_{off} ratio.

In our devices, the average I_{on}/I_{off} ratio can then be written as $\log\langle\frac{I_{on}}{I_{off}}\rangle = \log G_o^{on} - \log G_{off} \approx -6 + \log R_{off}$. This linear dependence is represented by the solid line in figure 3 and fits the data quite well.

We have performed similar statistical measurements on the low yield sample (wafer B: 3705 tested devices, 2% statistical uncertainty). For that sample, only 20% of the devices were connected (figure 4). Due to the lower methane proportion, fewer carbon species are present, which leads to a reduced yield of nanotube growth. However, the methane proportion difference between samples A and B is only 0.4%, while the electrical connection yields of the two batches differ by 66%. This shows the extreme sensitivity of the HFCVD process to slight parameter fluctuations, and the need for the accurate control of the deposition parameters. Interestingly, the semiconducting nanotubes were only p-type unipolar transistors. We attribute this to the different growth parameters that possibly favour SWNTs. The correlation linking R_{off} and the switching ratio I_{on}/I_{off} demonstrated on wafer A is also fulfilled in wafer B (dotted line in figure 5), but one notices that the standard deviation around this average law is much larger in batch B. Moreover, the metallic device occurrence is much larger than the semiconducting ones (6:1) and they also exhibit larger conductance fluctuations than for the metallic devices of wafer A. This suggests that a low yield sample with frequent single nanotube connection gives more dispersed conductance fluctuations with respect to a high yield sample for which the multiple connections in parallel already average the contact transparencies. This may reduce the number of high transparency connected semiconducting nanotubes.

These electrical statistics give insight into the reliability of the nanotube/metal self-assembled connection. The obtained statistics show that HFCVD is very powerful to connect carbon nanotubes by self-assembly, with a yield reaching up to 86%. However, this technique requires a precise control of the growth parameters as it is extremely sensitive to their fluctuations. We were able to correlate the measured resistances with the presence of metallic tubes connected in parallel with semiconducting ones, and to probe the nanotube–metal contact transparency fluctuations. Optimizing the growth step is a key point; however, good switching of the CNFETs is determined by a strong gate coupling as well. Top-gating of CNFETs [4] has been shown to provide turn-on voltages and transconductance better than state-of-the art silicon MOSFETs.

CNFET characteristics can be further adjusted by designing more sophisticated gate designs such as split gates [27], or by decreasing the gate oxide thickness [3]. This advanced gate fabrication can be easily integrated at the wafer scale. As a proof of concept, we show the effect of the gate dielectric thinning using low and high κ materials to design top gates at the wafer scale.

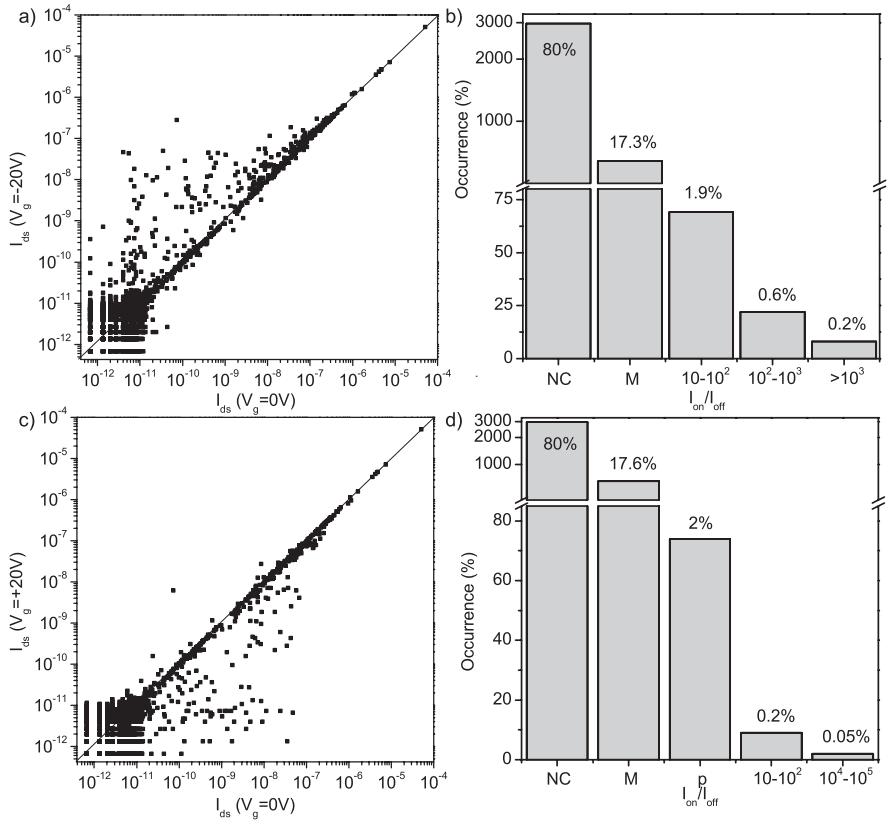

Figure 4. Statistics on as grown CNFETs distributed on a wafer having a low connection yield (wafer B). (a) Statistics for the p branch: the current in the p-branch *on* state ($V_g = -20$ V) is plotted versus the current in the *off* state ($V_g = 0$ V). The drain–source voltage is set at $V_{ds} = 100$ mV. The line is the frontier where both currents are equal. The points obtained below 10^{-11} A correspond to the detection limit of the set-up. (b) The statistics of (a) are plotted as a histogram versus the rate I_{on}/I_{off}. (c), (d) The same graphs for the n branch ($V_g = +20$ V).

We have thus focused on optimizing the gate effect by replacing back-gating by an efficient top-gating localized above the nanotubes. We have tried both low κ dielectrics (Parylene C) and high κ ones (HfO_2) as the gate dielectrics.

Parylene C is a polymer coating generated from derivatives of di-*para*-xylylene, widely used in the microelectronics industry. It has versatile use and easy deposition procedure: after being sublimed, the monomer spontaneously polymerizes on a cold surface, forming a uniform, conformal coating. Parylene C has a high dielectric strength (2.2 MV cm^{-1}, the average dielectric permittivity is $\varepsilon = 3.2$), high volume resistivity (8.8×10^{16} Ω cm), and excellent chemical resistance. It provides pinhole-free and conformal layers at the nanometre level as demonstrated for coating of nanotube terminated scanning probe microscopy tips [28] and organic transistor dielectric layers [29]. Conformal coating is particularly interesting in our case since free-standing SWNTs either isolated or in bundles can be kept suspended between the electrodes. Figure 6 shows a scanning electron microscopy (SEM) micrograph of as-fabricated CNFETs (a) and encapsulated ones in 20 nm of Parylene C by cold CVD (b). The CNTs connected to the electrodes appear thicker as they are conformally coated with Parylene but are still suspended over the substrate. A coaxial gate dielectric leading to gate coupling optimization [30] can be obtained in this case. After this step, a gold gate electrode is evaporated on top of the device and aligned above the inter-electrode gap of the transistor (as shown by the inset of figure 7). Parylene C is not soluble in most solvents, which allows using standard optical lithography (still a flash of oxygen plasma is needed to improve the metal adhesion on Parylene). We have tested the characteristics of devices covered with 100 nm of Parylene C in different gate configurations (figure 7). Parylene layers thicker than the one in figure 6(b) have been used for top-gating in order to avoid current leakage between drain–source and gate electrodes, and to minimize fluctuations due to the Parylene thickness variations at the wafer scale. Using the top gate, the *on*-state saturation current can be obtained at much lower gate voltage while the *off*-state current is dramatically decreased. This results in an I_{on}/I_{off} ratio enhanced by more than three decades [4] compared to those obtained by back-gating on the same device. Similarly, the gate swing $S = \frac{\partial V_g}{\partial \log I_{ds}}$ is decreased by a factor of three ($S = 720$ mV/decade) and the hysteresis (not shown here) almost disappeared in top gating. Using top and back gates simultaneously further enhanced the switching performance of the device (triangles in figure 7). Reduced gate dielectrics alone cannot account for this improved performance, and one can attribute the enhanced gating to a higher electric field distribution near the Schottky barriers localized at the nanotube/metal contact as predicted in [30, 31]. Such an enhanced electric field distribution is likely caused by the peculiar geometry caused by the finger-like shape of both the titanium/nanotube contacts and the top gate, which fits the nanotube channel length (inset figure 7).

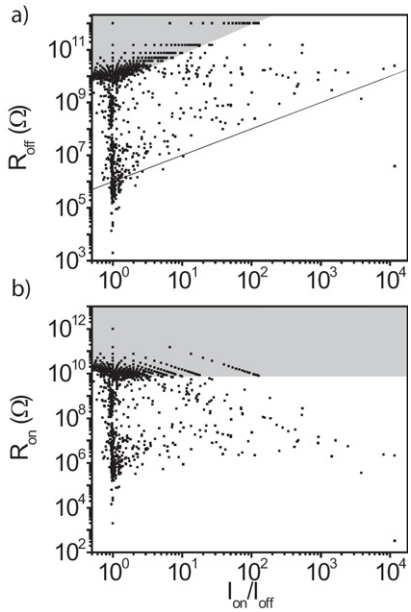

Figure 5. (a) Resistance in the *off* state for wafer B plotted versus the *on*-to-*off* current ratio. The line corresponds to the calculated R_{off} with our model. (b) The same for resistance in the *on* state. In both cases, the grey zones correspond to the detection limit of the set-up.

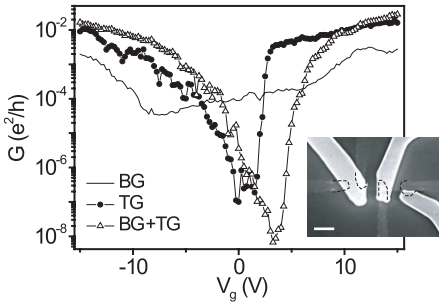

Figure 7. Transfer characteristics of a typical fully integrated CNFET (wafer A) using a 20 nm thick Parylene C layer as the gate dielectrics. The drain–source voltage was 100 mV. The measurements were performed at room temperature, under a pressure of 10^{-6} mbar, and for a sweep rate of -150 mV s^{-1}. The transfer characteristics were successively measured using the back gate (BG, plain line), the top gate (TG, black dots), and both of them (empty triangles). The inset is an electron micrograph of the fully processed circuit showing the top-gate finger electrodes (bright areas) aligned over the gaps between titanium electrodes (dotted contours) (scale bar = 1 μm).

Furthermore, we have checked that the Parylene encapsulation is fully compatible with functionalized CNFETs, especially for nanotubes coupled to gold nanoparticles, which have been shown to behave as single electron memories [32].

A study involving hafnium oxide (HfO_2) as the gate dielectric has also been realized. This material is known to give nearly ideal sub-threshold slope when used as a gate dielectric for CNFETs [33]. Its dielectric permittivity ranks this material among the high κ dielectrics which are suitable materials for high efficiency gating. HfO_2 deposition was performed at 360 °C by liquid injection metallorganic chemical vapour deposition [34, 35]. The precursor was $Hf(OtBu)_2(mmp)_2$ dissolved in octane (0.05 M). Attenuated total reflection Fourier transform infrared spectroscopy confirmed the amorphous nature of the films. The HfO_2 thickness for this study was 5.8 nm as calculated from the x-ray reflectometry measurements made on a Si/SiO_2 (0.8 nm) reference substrate put in the chamber together with the sample. In these deposition conditions, the dielectric permittivity is typically about 22. A typical result on our CNFET is shown in figure 8. This material allowed us to obtain a p-type field effect exhibiting a sub-threshold slope of about 170 mV/decade, which is better than with Parylene C and in very good agreement with the prototype of HfO_2 top-gated devices of similar geometry [27]. However, this material was found to be more difficult to integrate than Parylene C, mainly because instabilities in the channel current were found upon gating.

Finally, we present a low temperature measurement of Parylene coated devices that exhibit stable ambipolarity with optimized field effect characteristics. Figure 9 shows the transfer characteristics at $T = 6$ K of an ambipolar CNFET encapsulated in 100 nm of Parylene C. This device exhibits a very sharp threshold region characterized by $S = 200$ mV/decade and seven decades of current switching amplitude. At the threshold between *on* and *off* states, the device presents conductance fluctuations due to Coulomb blockade (see supplementary information of [32]). Similar effects together with a detailed study of the temperature dependence of back-gated HFCVD CNFETs, showing a saturation of S upon cooling due to thermally activated tunnelling, can be found in [20].

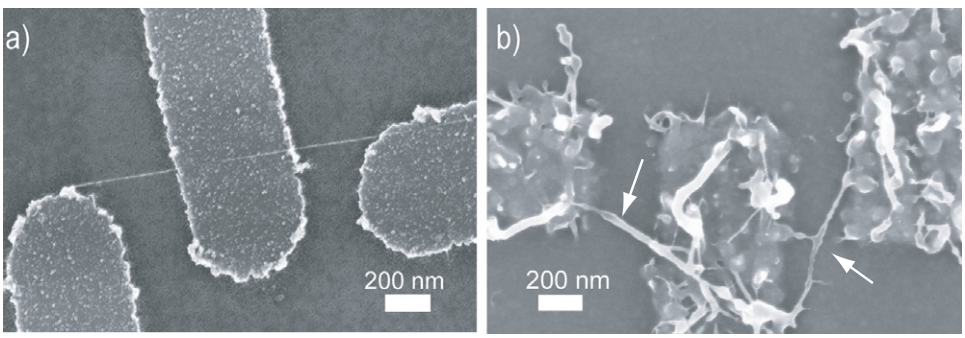

Figure 6. SEM micrographs showing (a) an as grown CNFET and (b) a typical CNFET after deposition of a 20 nm thick Parylene C layer. A conformal coating recovers the nanotube channels (arrows).

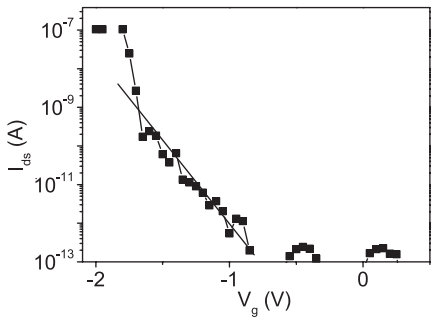

Figure 8. Typical transfer characteristics of a top-gated CNFET using a 6 nm thick layer of HfO_2 as the gate dielectric. The drain–source voltage was 100 mV. The measurements were performed at 300 K in air, and for a gate sweep rate of -125 mV s^{-1}. The curve was measured using both top and back gates. The linear fit in the threshold region is shown as a plain line and gives a gate swing $S = 170$ mV/decade. The saturation at $I_{ds} = 10^{-7}$ A is due to the current compliance, that was set at this value to protect the device.

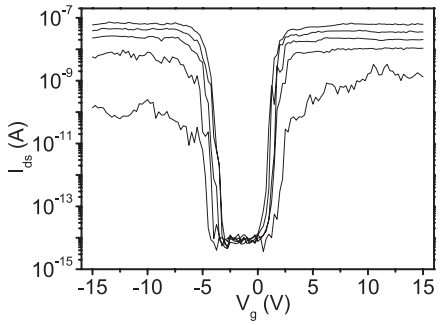

Figure 9. Top gate transfer characteristics of a CNFET using a 100 nm thick Parylene layer as the top gate dielectric. The measurement was performed at $T = 6$ K, with both top and back gates polarized with gate sweep rate of -100 mV s^{-1}. The drain–source voltage is increased by 100 from 100 to 500 mV from bottom to top.

4. Conclusion

In conclusion, we have performed statistical electrical measurements on nanotube-based devices. These statistics show the reliability of our self-assembled integration, which can reach up to 86% of operational devices. We observe a stable ambipolar field effect for half of the semiconducting devices and we attribute this effect to the high occurrence of double walled carbon nanotubes generated by our peculiar CVD growth. Moreover, the statistics on the conductance of the device reveal a general evolution related to the presence of weakly coupled metallic nanotubes. This allows us to quantitatively address the dispersion of the device characteristics and to correlate them with the growth parameters. We have shown that our device characteristics can be further improved by increasing the gate coupling. We have designed a local top gate which can be implemented at the wafer scale. By using low and high κ dielectrics, we have increased the field effect of our devices and obtained gate swings down to 170 mV/decade. This work shows that batch characterization and processing of molecular devices opens the way to large scale integration and provides a step beyond the prototyping stage.

Acknowledgments

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