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Solid-State Electronics 49 (2005) 1497–1503
SOLID-STATE ELECTRONICS
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Field effect and Coulomb blockade in silicon on insulator nanostructures fabricated by atomic force microscope

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Available online 12 September 2005

The review of this paper was arranged by Prof. F. Gamiz

Abstract

The comprehensive understanding of the electrical behaviour of silicon nanostructures becomes more and more important for the evolution of the microelectronics towards nanoelectronics. In this context, we present a complete bench test for the study of silicon nanostructures, from the fabrication by a non-conventional technique, to the electrical characterisation at room and low temperature. Nanostructures with lateral gates are fabricated with an atomic force microscope (AFM) on silicon on insulator (SOI) substrates. At room temperature, we demonstrate a field effect transistor-like behaviour due to the backgate and also to the lateral gate. At low temperature, the electrical transport is a superimposition of the field effect and single-electron phenomena (Coulomb blockade). We demonstrate the one-dimensional character of the electrical transport at low temperature using a theoretical model for arrays of dots.

Keywords: AFM lithography; SOI; Silicon nanostructures; Field effect; Coulomb blockade; One-dimensional electrical transport

1. Introduction

The trend in microelectronics is to reduce the dimension of the devices. In this context, nowadays, there is a real crossing from microelectronics to nanoelectronics and two types of problems are brought up: difficulties of fabricating the structures and understanding the new transport phenomena that may appear in very low-scale devices.

From the fabrication point of view, the limits of optical lithography techniques are more and more obvious, in terms of resolution, flexibility, cost etc., so, new approaches are needed. Atomic Force Microscopy (AFM) based lithography is one of the most promising alternative techniques that emerges. Typically, AFM is used to image the surface of a sample, by scanning a tip onto the surface. The tip may induce changes in the surface in very precise conditions (for example by applying a potential between the tip and the scanned surface), so AFM can become a high resolution lithography tool.

The first description of nanostructures fabrication by AFM lithography on SOI substrates was described by Campbell et al. [1]. The refinements of this method, such as the oxidation in tapping mode [2] or the use of a pulsed tension on the tip [3], have improved the lateral resolution of the structures designed. Later

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0038-1101/$ - see front matter © 2005 Elsevier Ltd. All rights reserved.
doi:10.1016/j.sse.2005.07.012

developments of this technique on SOI substrates are presented in Refs. [4,5].

The scientific groups that are working on silicon nanowires are typically specialised either in the fabrication or in the study of the electrical transport. The main advantage of our work is that we do fabrication by a flexible technique and electrical transport measurements at room and low temperature.

The structures presented in this paper are fabricated using the AFM lithography in contact mode with a pulsed-biased-tip. In order to reveal silicon nanostructures an etching step is necessary. The use of SOI substrates is compulsory because the buried oxide layer acts as an etch stop layer. Moreover, the use of SOI ensures high quality interfaces and reproducible electrical properties of the structures, as demonstrated in this article.

Electrical transport at room temperature shows a field effect due to the backgate. This field effect can be well described by the existing SOI models. A field effect due to the lateral gates is also evidenced.

At low temperature, the conduction through the nanostructures is a superposition of the field effect and of Coulomb blockade phenomenon. A model of the transport through an array of dots allows demonstrating that the nanowires act mainly as uni-dimensional structures at low temperatures.

2. Fabrication

We have chosen to use the oxidation by AFM in contact mode. The fabrication steps [6] are schematically presented in Fig. 1.

The substrates used are Unibond® SOI [7] samples with an ultra-thinned monocrystalline Si layer down to 15 nm and with a 400 nm buried oxide thickness. The samples are doped with Arsenic and we dispose of two doping levels, 10^{17} cm^{-3} and 10^{19} cm^{-3}. Electrical connections are provided by 80 nm thick pads made of degenerately doped silicon.

The first step is to dip the SOI substrates in a HF (2% water solution) for 1 min. This treatment has two aims: removing the native oxide naturally existing on the wafer surface and passivating the silicon layer by a metastable hydrogen terminated surface. During this step the Si–O bonds are replaced by low energy Si–H bonds.

The second step consists in the anodisation of the Si–H surface under negatively biased tip. Previous studies showed that there is a threshold voltage of −2.7 V [8,9] in order to break the Si–H bondings and to induce the oxidation of the surface under the tip. A very important parameter is the humidity; we need to have a level of about 30–40%. This humidity level forms a water meniscus between the tip and surface. The anodisation reaction takes place in this water meniscus. The scan speed of the tip is fixed to 0.1 μm/s during the AFM lithography. Typical dimensions of the oxide patterns obtained with these parameters are of 0.5–1.5 nm in height and about 30–70 nm in width [10]. Fig. 2 shows an oxide mask drawn by AFM lithography.

The good chemical contrast between the Si surface and the AFM drawn oxide permits a silicon wet etching

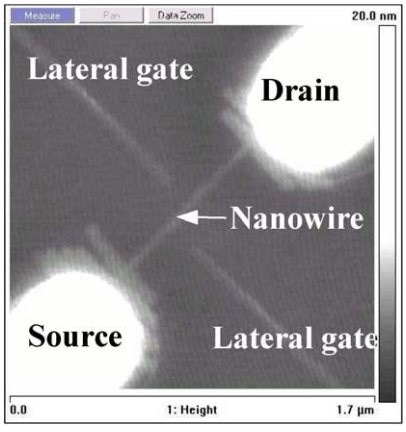

Fig. 2. AFM image of the oxide mask drawn by AFM lithography. In this example the oxide wire is about 750 nm in length, 40 nm in width and 1 nm in high. The asymmetric lateral gates are at 120 nm and 130 nm away from the channel.

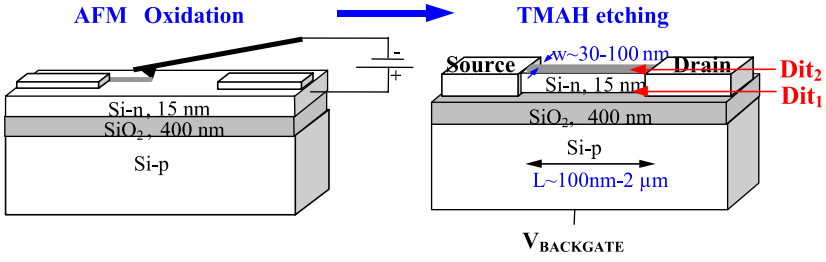

Fig. 1. Schematic of the fabrication steps: AFM local oxidation between the existing contacts of the SOI substrate, followed by the wet etching of the silicon in order to obtain the final silicon nanostructure (with the interface state densities Dit_1, between the Si top layer and the buried oxide and Dit_2, between the silicon layer and the native oxide). Typical dimensions of the final structures are: 100 nm–2 μm in length, 30–100 nm in width and 15 nm thickness.

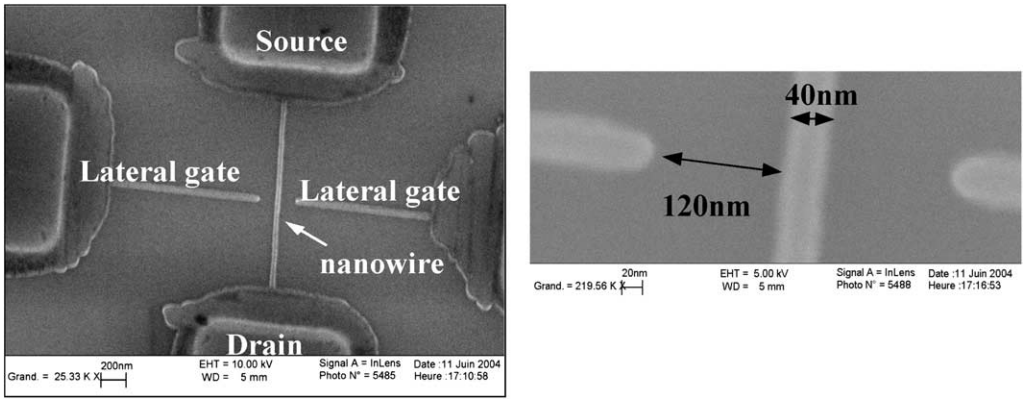

Fig. 3. Scanning electron beam image of a final structure. Here, the dimensions are $L = 1.2$ μm, $w = 40$ nm, $h = 15$ nm and the channel-gate gap of 120 nm, which corresponds to a cross-section of 600 nm^2. The dopant level is of 10^{17} cm^{-3}, so the inter-dopant distance is about 20 nm. This means that there is an average of one dopant per cross-section.

step. We use tetramethyl-amino-hydroxide (TMAH) to ensure a very high selectivity ratio between Si/SiO_2 (etch rate 2000:1) [11]. Fig. 3 shows a scanning electron microscope image of a final structure. Considering the dimensions and the doping level of the structure, we have estimated that there is only one dopant per cross-section.

Electron-beam lithography would allow reaching the same kind of resolution but during the process, highly energetic electrons are introduced in the devices and they can damage the crystalline structure of the silicon. Furthermore, the pitch between the structures made by e-beam lithography is limited by proximity effects. The main advantage of AFM lithography is that it involves low energy electrons emitted in the near-field regime. This implies that the resolution is not affected by diffraction or proximity effects moreover it is a non-invasive technique.

The AFM lithography on SOI substrates is a resist-less technique for fabricating surface silicon nanostructures. As the oxide mask is made by direct writing with the AFM tip on the silicon top layer. It is easy to change the geometry of the designed oxide, which makes the AFM an ideal tool to fabricate nanostructures.

3. Field effect in the silicon nanostructures

The nanostructures fabricated were tested in order to investigate their electrical behaviour at room temperature. The nanowires can be compared to the channel of a field effect transistor. However, as their dimensions—thickness and width—are very small the reproducibility of their electrical properties and their FET behavior is not trivial.

Firstly we are demonstrating that at room temperature and for nanostructures fabricated with the same lithographic parameters lead to similar electrical characteristics. Fig. 4 presents I_{DRAIN}–V_{DRAIN} curves for the two identical structures (1 μm in length, 15 nm in height,

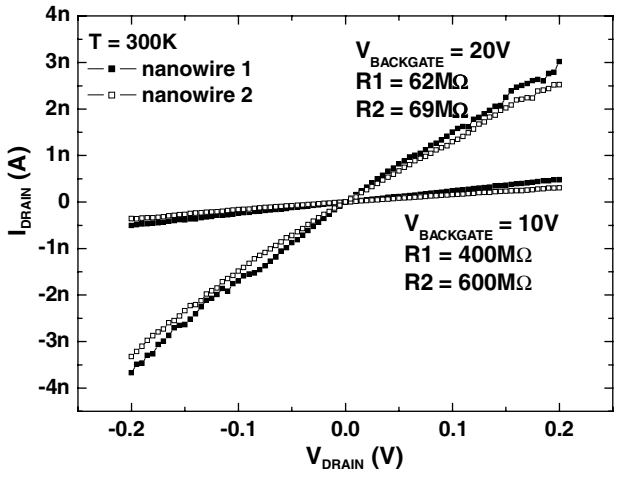

Fig. 4. I_{DRAIN}–V_{DRAIN} curves for two structures (□) and (■) fabricated with the same parameters. The resistances of the two nanowires, R_1 and R_2, estimated as the slope at origin of the current curves have similar values in two different regimes (accumulation, $V_{BACKGATE} = 20$ V and desertion, $V_{BACKGATE} = 10$ V) and are thus demonstrating the good reproducibility of the electrical properties at room temperature.

70 nm in width and a doping level of 10^{19} cm^{-3}). The curves are superposed for two different backgate voltages corresponding to the accumulation (20 V) and to the depletion (10 V) regimes. We notice that we need to apply a voltage on the backgate in order to suppress the space charge region naturally existing in the nanowire. This experiment shows that, at room temperature, the fluctuation of the number of dopant atoms does not affect the electrical properties. This reproducibility of the electrical properties versus lithographic parameters was not reported before.

Fig. 5 gives the I_{DRAIN}–$V_{BACKGATE}$ characteristics for a nanowire of 800 nm in length, 70 nm in width, 15 nm in height and with a dopant level of 10^{17} cm^{-3}. The curves in Fig. 5(a) represent the measurements done on fresh samples. The subthreshold swing, S, was

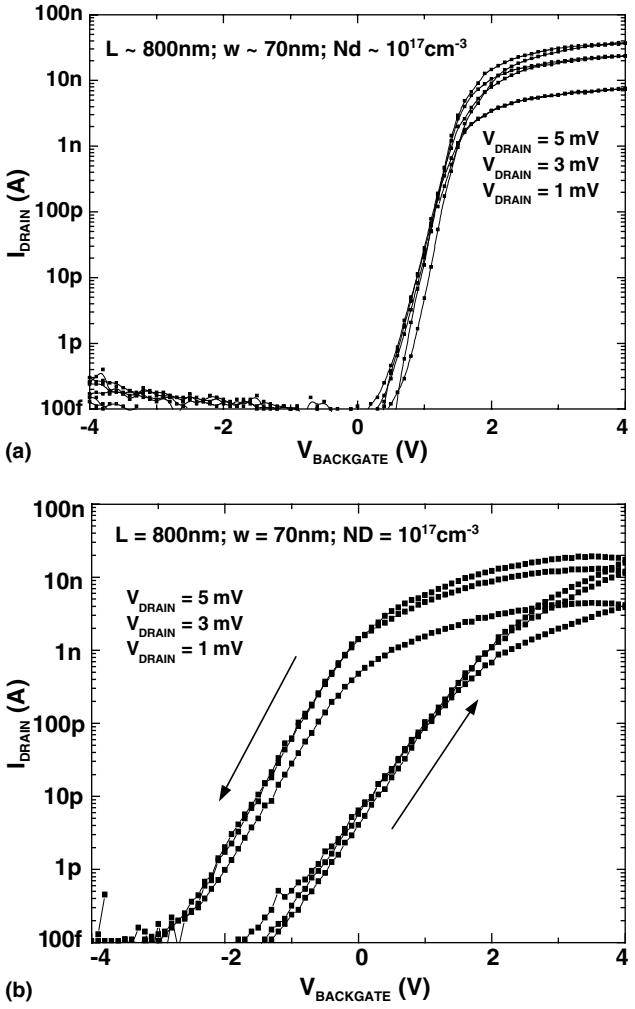

Fig. 5. The curves I_{DRAIN}–V_{BACKGATE} at 300 K are showing the field effect due to the backgate. The structure under test has a doping level of about $10^{17}\,\mathrm{cm}^{-3}$, $L \sim 800$ nm, $w \sim 70$ nm, $h \sim 15$ nm. The curves in (a) are measurements realised directly after the fabrication. They are showing a very small hysteresis (0.1 V) and a swing $S \sim 200$ mV/decade. The curves in (b) are measurements done three weeks later. They are showing a strong hysteresis (1.4 V) and a swing $S \sim 750$ mV/decade. The difference between the two measurements is associated to the growth of the native oxide layer on the structure.

estimated to about 200 mV/decade. It is important to note that a very weak hysteresis (0.1 V) is present on theses curves. The curves in Fig. 5(b) present the measurements on the same structure but three weeks later. The new subthreshold swing is estimated at 750 mV/decade and the curves present a large hysteresis (1.4 V). We can evaluate the swing by using a model for thin SOI films that takes into account the potential contribution of the native oxide interface [12]:

$$S \cong \frac{\ln(10)}{C_{\mathrm{ox}}} \cdot \left(\frac{q}{k_{\mathrm{B}} \cdot T} - \frac{1}{E_{\mathrm{F}} \cdot t_{\mathrm{Si}}} \cdot \frac{C_{\mathrm{it2}}}{C_{\mathrm{Si}} + C_{\mathrm{it2}}} \right)^{-1} \cdot \left(C_{\mathrm{ox}} + C_{\mathrm{it1}} + \frac{C_{\mathrm{Si}} \cdot C_{\mathrm{it2}}}{C_{\mathrm{Si}} + C_{\mathrm{it2}}} \right) \quad (1)$$

where C_{ox} is the capacitance of the buried oxide, E_{F} is the electric field at the Si—buried oxide interface, t_{Si} is the thickness of the top silicon layer, C_{it1} is the capacitance due to the interface state density between the top silicon and the buried oxide, C_{it2} is the capacitance due to the interface state density between the top silicon and the air.

The native oxide layer will not contribute to S for the electrical tests on fresh samples, so $C_{\mathrm{it2}} = 0$. For a top silicon thickness of 15 nm and an interface state density silicon—buried oxide of about $5 \times 10^{10}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ Eq. (1) gives:

$$S_{\mathrm{no\_native\_oxide}} \approx 100\ \mathrm{mV/decade}$$

When the native oxide layer is formed, the interface top Silicon – air and C_{it2} become important. The interface state density between the silicon and the native oxide is about $10^{12}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ [13]. In this case, we obtain for the swing:

$$S_{\mathrm{with\_native\_oxide}} \approx 1\ \mathrm{V/decade}$$

Trapping and detrapping phenomena take place in the native oxide layer. Therefore, the evolution of the hysteresis might be also linked to the presence of the native oxide layer. Additional characterisations are in progress to investigate in more details the origin of this hysteresis.

A typical I_{DRAIN}–$V_{\mathrm{LATERALGATE}}$ curve is given in Fig. 6. Even if the lateral gates are very small and their effect on the wire is very localised, there is a field effect due to the polarisation on the lateral gates.

At room temperature the nanostructures have reproducible electrical properties and the fluctuations of the number of the doping atoms do not affect these properties. The conduction through the wire is modulated by the voltage applied on the backgate. The classical models of SOI are still valid for the electrical properties of the silicon nanostructures. As there is also a field effect

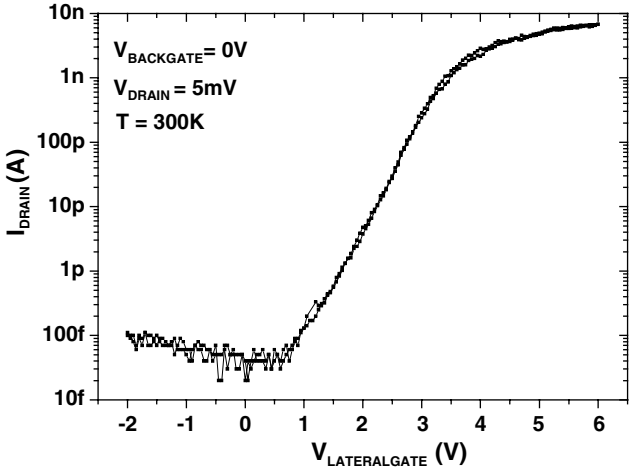

Fig. 6. I_{DRAIN}–$V_{\mathrm{LATERALGATE}}$ curve of a typical silicon nanowire showing the field effect due to the lateral gate.

due to the lateral gate, this means that the nanostructures act as multi-gate field effect transistors at room temperature.

4. Coulomb blockade in silicon nanostructures

The electrical properties of the nanostructures at low temperature were also studied. We want to see if the field effect is still present and if other phenomena are revealed.

In I_{DRAIN}–$V_{BACKGATE}$ curves (Fig. 7(a)) clear oscillations are superimposed with the field effect. Two measurements were done from low backgate voltage to high backgate voltage and other two the reverse way. The peaks obtained in the four curves are superposed; they represent the Coulomb blockade phenomenon. The origin of the Coulomb blockade in highly doped silicon nanostructures is related to the potential fluctuations around the dopant atoms [14]. For low temperature measurements, the local potential fluctuations are more important than the thermal energy and their influence becomes predominant in the electrical characteristics.

The most simple structure to obtain Coulomb oscillations is a single dot connected to source and drain by tunnel barriers. In this case, with the hypothesis that there can be only one extra electron in the dot, the capacitance of the dot with respect to the gate can be estimated from the peak to peak distance [15]. Furthermore, the diameter of the dot can be evaluated. In the Fig. 7(a), the peak to peak distance is of about 2 V. For the case of a single dot charged with a single electron, the capacitance is about 0.1 aF. A simple model of a planar capacitance between a disc (the dot) and a plane (the bulk silicon), as shown in the schematic in Fig. 7(b), allows estimating the radius of the dot to about 13 nm. As we suppose that the Coulomb blockade originates from the potential fluctuations due to the doping atoms, this radius should have the same order of magnitude as the average distance between two dopant atoms. The nanostructure under test has a doping level of about $10^{17}\,cm^{-3}$, which corresponds to an inter-dopant distance of about 20 nm. It is possible that not all the doping atoms are electrically active, so it is understandable that the dot-diameter estimated from the electrical measurements is slightly larger than the inter-dopant distance, but the order of magnitude for the two parameters is the same. Anyway the coherence between the two parameters confirms the hypothesis that the Coulomb blockade phenomenon is due to the potential fluctuations around the doping atoms.

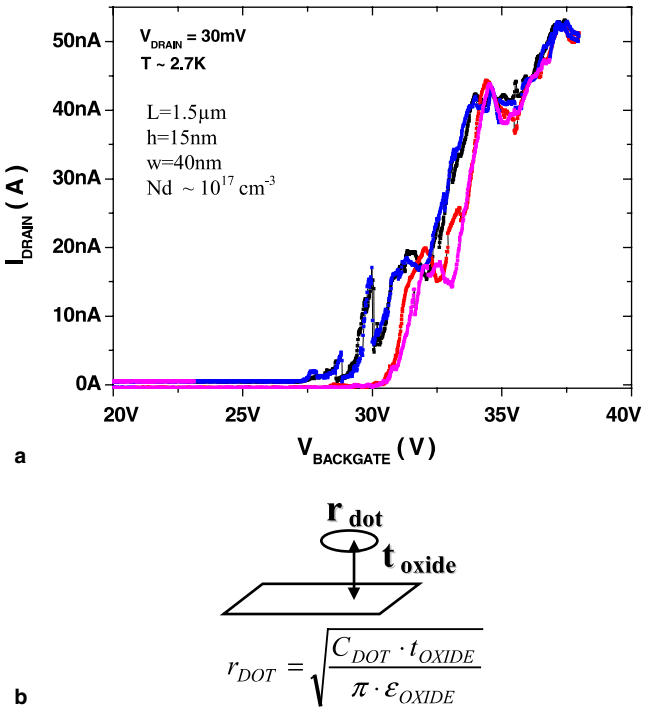

Fig. 7. (a) I_{DRAIN}–$V_{BACKGATE}$ curves at low temperature (2.7 K). Reproducible Coulomb oscillations are superimposed to the field effect still present at low temperature. (b) Schematic of a simple model of planar capacitance. The radius of the dot where the Coulomb blockade is taking place can be estimated.

A convenient way to present the electronic properties at low temperature is to map the drain current versus the backgate voltage and the drain voltage. This map, also called stability diagram, exhibits some rhombus, or Coulomb diamonds, corresponding to the blocked state of the device. For the ideal case of a single dot the Coulomb diamonds are regular [15]. In Fig. 8, the stability diagram obtained on one of our nanostructures has non-regular Coulomb diamonds. There are two phenomena responsible for this irregularity. On one hand, the dimensions of the potential wells in the device are not fixed, but they depend on the backgate voltage applied, as shown in Fig. 9. These potential wells around the dopant atoms are similar to dots where the electrons are spatially localised. Potential barriers are present between two dots and electrons may tunnel from one dot to the other. When the backgate voltage is increased, the energy barrier between two doping atoms becomes smaller therefore the electronic transport through the nanostructure is established easier. Furthermore the diameter of the dots can also increase with the backgate voltage, so the thickness of the tunnel barriers decreases. Therefore both the height and the thickness of the tunnel barriers between dots decrease when the backgate voltage increases. The blocked regions must be smaller for high backgate bias. This is exactly what we can see in the stability diagram (Fig. 8): the Coulomb diamonds are smaller for high backgate potentials. One the other hand, the diamonds structure is not simple (each diamond seems to have a double peak) which implies that the nanowire cannot be modeled by a single dot. A more adapted theoretical model corresponds to an array of dots, having different dimensions (Fig. 9).

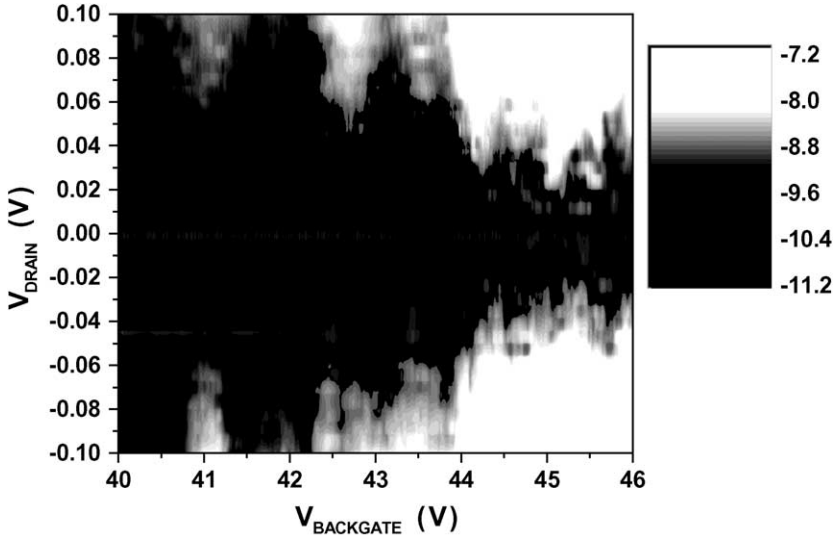

Fig. 8. Map of the drain current (in logarithm scaling) as a function of the backgate voltage (x-axis) and the drain voltage (y-axis) at 4.2 K. The Coulomb diamonds visible here are not regular because of the superposition with the field effect and also because the structure is more complex than a single dot.

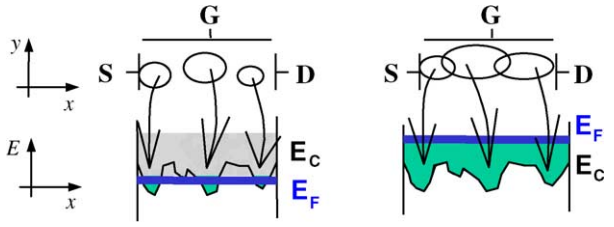

Fig. 9. A more adapted model for the nanostructures is an array of potential fluctuations around the doping atoms. The dimensions of these potential wells are modified by the backgate voltage.

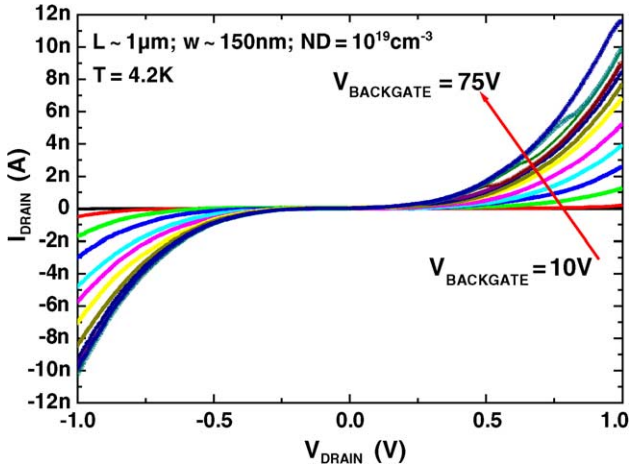

Fig. 10. I_{DRAIN}–V_{DRAIN} curves showing a zero-conductance region. This region is modulated by the bias applied on the backgate.

Fig. 10 presents the I_{DRAIN}–V_{DRAIN} curves and their dependence with the backgate voltage. We notice a zero-conductance region around $V_{DRAIN} = 0$ V, which corresponds to the blocked regions in the stability diagram.

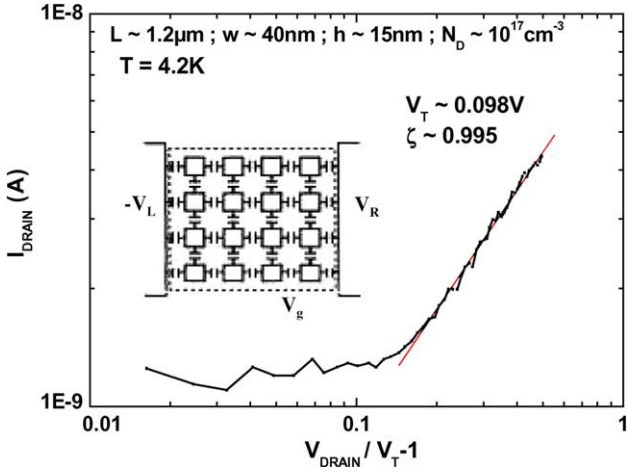

Fig. 11. I_{DRAIN}–$(V_{DRAIN}/V_T - 1)$ curve for a nanostructure with a doping level of 10^{17} cm^{-3}. A model of capacitively coupled dots (shown in the inset [16]) allows estimating the dimensionality of the array. The slope of the curves is 1 for a 1D system and 5/3 for 2D systems. From our measurements the slope corresponds to about 1.

The zero-conductance region is modulated by the backgate voltage.

A theoretical model presented in [16,17] and based on arrays of capacitively coupled dots (inset of Fig. 11) shows that the current through such an array has a power law dependence with the drain voltage:

$$I_{DRAIN} \propto \left(\frac{V_{DRAIN}}{V_{THRESHOLD}} - 1\right)^{\zeta} \quad (2)$$

The scaling factor, ζ, depends on the dimensionality of the array: $\zeta \sim 1$, for one-dimensional array and $\zeta \sim 5/3$ for two-dimensional array. We have applied this model to our experimental data (Fig. 11). The scaling

factor was estimated between 0.9 and 1.1. We conclude that the nanowire at low temperature has a one-dimensional array electrical behaviour, which is consistent with the fact that there is an average of one doping atom occupying the cross-section of the wire.

5. Conclusion

Good theoretical and experimental backgrounds are needed for the future development of nanoelectronic devices. We present here a fabrication method together with the electrical measurements (at room and low temperature) of silicon nanostructures.

The non-conventional fabrication method used is based on AFM lithography of ultra-thin highly doped SOI substrates. The final structures are silicon nanowires with lateral gates. The monocrystallinity and the high quality interfaces of the SOI substrates lead to the fabrication of nanostructures with reproducible electrical properties.

The electrical tests at room temperature show a multi-gate transistor-like behaviour that can be understood with the existing SOI models.

At low temperature the nanostructures show strong and reproducible Coulomb oscillations superposed on the field effect. We show that the origin of the Coulomb blockade is linked to the potential fluctuations due to the presence of doping atoms in the wires. From the electrical transport point of view, the nanowires behave like one-dimensional arrays of capacitively coupled dots. This conclusion is consistent with the fact that typically there is only one doping atom occupying the cross-section of the structures.

Our future studies shall be concentrated on the evolution of the electrical properties from room temperature to low temperature. Possible evolution of the scaling factor, ζ, with the temperature is in progress.

Acknowledgements

The authors are grateful D. Fraboulet, D. Mariolle and J. Gautier from LETI/CEA Grenoble for providing the ultra-thin SOI substrates.

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